500mA Single-Cell Li-ion Battery Charger with Power Path Management, 1mA Termination and 1uA battery leakage current

small battery capacity

1. FEATURES

- Input voltage range 3.6V-6V, 23V Maximum input surge voltage.
- Support the charging target voltage is 3.6V ~ 4.55v for Li-Ion/Polymer Batteries
- ±0.5% Charging Voltage Accuracy
- Bidirectional true shutdown from VIN to VSYS and from VBAT to VSYS
- Dynamic power management (DPM) function for Input voltage and current
- IP2333_I2C supports I2C interface for Setting Charging Parameters and Status Reporting
- Up to 500mA charging current
- Minimum 1 mA EOC current
- VDD output with 20mA current capacity
- Support NTC detection of battery temperature for JEITA standard charging
- Ultra low power consumption mode, the BAT leakage current is less than 1 μ A
- Charging status and fault status indication
- Perfect charging protection functions include: input over voltage, battery over voltage, IC over temperature, NTC low and high temperature, charging timer monitoring, thermal limiting regulation on-chip, battery discharge over current protection and system short circuit protection
- In shipping mode of IP2333_I2C, leakage current is less than 400nA
- DFN8(0303) package

2. APPLICATIONS

- TWS
- Wearable Devices
- Bluetooth audio and other portable devices with

3. DESCRIPTION

The IP2333 is a highly integrated, ultra low VBAT leakage current single-cell Li-ion/Li-polymer battery charger with system power path management for space-limited portable applications.

The charger function features includes of Trickle-charge (TC), fast current (CC) and constant voltage (CV) regulation, charge termination, and auto-recharge. The IP2333 takes input power from either an AC adapter or a USB port to supply the system load and charge the battery simultaneously. The power path management function ensures continuous power to the system by automatically selecting the input, battery, or both to power the system. Power path management separates the charging current from the system load, which allows for proper charge termination and keeps the battery in full-charge mode. The IP2333 provides a system short-circuit protection (SCP) function by limiting the current from the input to the system and the battery to the system. This feature is especially critical for preventing the Li-ion battery from being damaged due to an excessively high current. An on-chip battery under-voltage lockout (UVLO) cuts off the path between the battery and the system if the battery voltage drops below a programmable battery UVLO threshold. This prevents the Li-ion battery from being over-discharged. An integrated I^2C control interface allows the IP2333_I2C to program the charging parameters, such as input current limit, input minimum voltage regulation, charging current, battery regulation voltage, safety timer, and battery UVLO.

IP2333 VDD power supply up to 20mA load current. The IP2333 is available in a DFN8 (0303) package.

4. TYPICAL APPLICATION

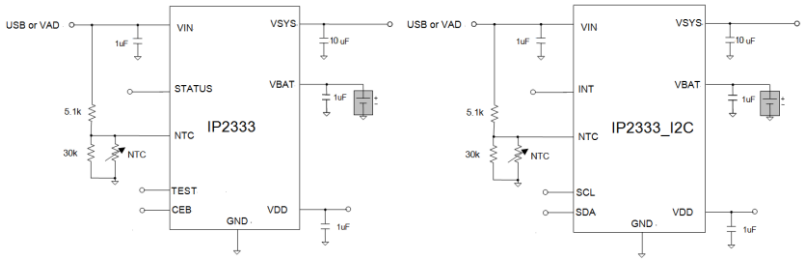


Fig1 IP2333 and IP2333_I2C Typical Application

5. PACKAGE REFERENCE

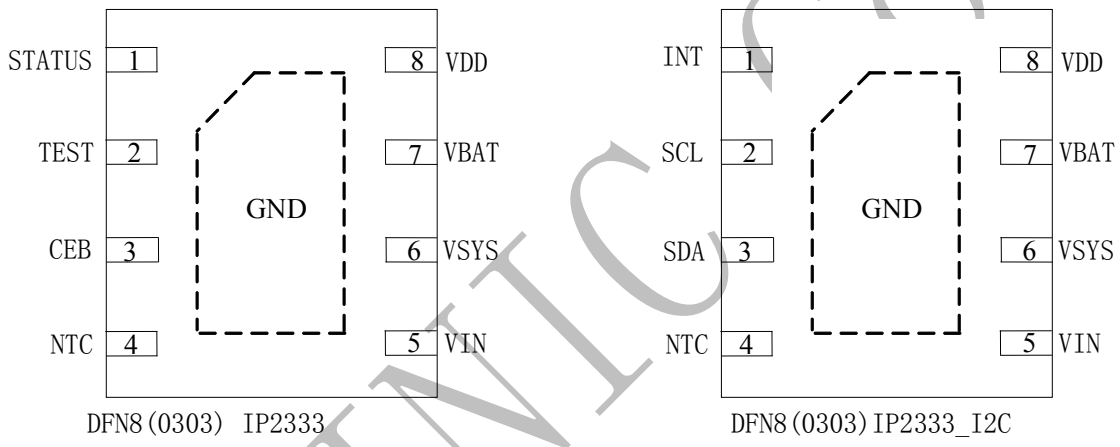


Fig2 IP2333 pin function

IP2333 PIN FUNCTIONS:

Pin No.	Pin name	Function description
1	STATUS	Status display pin. Open drain output, LED connected to the VIN for indicate charging/fault status.
2	TEST	Connect to VBATwith 1kohm resistor
3	CEB	Charging enable pin. Low level active, internal 10Mhm pull-down resistance. If VIN input does not exist, this pin is invalid.
4	NTC	Temperature sense input. Connect a negative temperature coefficient thermistor to NTC. Program the hot and cold temperature window with a resistor divider from VIN to NTC to GND. Charging is suspended when NTC is out of the range. It is recommended to connect NTC resistance of ncp18XH103, B25/50=3380K. It can't be float; replace it with normal temperature resistance if NTC function is not used.
5	VIN	Input power pin. Place a ceramic capacitor from VIN to GND as close to the IC as possible.
6	VSYS	System power supply. Place a ceramic capacitor from VSYS to GND as close

		to the IC as possible.
7	VBAT	Battery pin. Place a ceramic capacitor from BATT to GND as close to the IC as possible.
8	VDD	VDD LDO supply. The maximum load capacity is 20mA
EPAD	GND	Ground.

IP2333_I2C PIN FUNCTIONS:

Pin No.	Pin name	Function description
1	INT	Interrupt output. INT can send a charging status and fault interrupt signal to the host. INT is also used to disconnect the system from the battery and VIN to reset system.
2	SCL	I2C interface clock.
3	SDA	I2C interface data.。
4	NTC	Temperature sense input. Connect a negative temperature coefficient thermistor to NTC. Program the hot and cold temperature window with a resistor divider from VIN to NTC to GND. Charging is suspended when NTC is out of the range. It is recommended to connect NTC resistance of ncp18XH103, B25/50=3380K. It can't be float; replace it with normal temperature resistance if NTC function is not used.
5	VIN	Input power pin. Place a ceramic capacitor from IN to GND as close to the IC as possible.
6	VSYS	System power supply. Place a ceramic capacitor from SYS to GND as close to the IC as possible.
7	VBAT	Battery pin. Place a ceramic capacitor from BATT to GND as close to the IC as possible.
8	VDD	VDD LDO supply. The maximum load capacity is 20mA, I^2C can set to turn off VDD output.
EPAD	GND	Ground.

6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
High voltage pin input voltage range	VIN, STATUS/INT，NTC	-0.3V to 23	**V**
Low voltage pin input voltage range	SCL,VDD，SDA, CEB,LPB,VSYS,VBAT	-0.3V to 6	**V**
Junction temperature	T_J	-40 ~ 125	℃
Storage temperature	Tstg	-60 ~ 150	℃
Thermal Resistance	θ_{JA}	70	**℃/W**
Human body model（HBM）	ESD	2	**KV**

* Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7. Recommended Operating Conditions

Parameter	Symbol	MIN.	NOM.	MAX.	Unit
input voltage range	VIN	3.6	--	6	V
Operating free-air temperature range	T_A	-40	--	85	℃

* The device is not guaranteed to function outside of its operating conditions.

8. IC type List

Type	Pin No.	Pin Function	Description
IP2333	1	STATUS, open drain output.	GPIO set charging enable or not. The charging status can be output through STATUS pin.
	2	TEST, pull up to VBAT with 1kohm resistor	
	3	CEB, As GPIO setting input.	
IP2333_I2C	1	INT, Interrupt output	I^2C can set register parameter. Status flag can be reported by the interrupt pin.
	2	SCL, I^2C clock	
	3	SDA, I^2C data	

9. ELECTRICAL CHARACTERISTICS

Unless otherwise noted， T_A = -40° C to 85°C. Typical values are for T_A = 25ºC.VIN = 5 V, NTC = 3 V, VBAT =3.6V.

Parameter	Symbol	Test condition	MIN.	NOM.	MAX.	Unit
Input VIN and output VSYS characteristics						
Input voltage range	VIN		3.6	5	6	V
Input quiescent current	I_Q	VIN=5V		1	2	mA
VIN OVP	VIN_{OVP}	VIN rise	5.8	6	6.2	V
	VIN_{OVP_HYS}	VIN fall	150	200	250	mV
VIN UVP	VIN_{UVLO}	BAT=3V, VIN rise	3.60	3.70	3.85	V
	VIN_{UVLO_HYS}	BAT=3V, VIN fall	3.5	3.55	3.7	V
VIN-DPM threshold	VIN-DPM	Register default value: 4.32V	4.22	4.32	4.42	V
VSYS voltage value	VSYS	Register default value: 4.65V	4.55	4.65	4.75	V
AFET on resistance	$AFET\_R_{DSON}$	ISYS=0.5A，VIN=4.4V		200	300	mohm
Input current limit	ILIMIT		50	-	500	mA
	ILIMIT_ACC	Register default value=0.5A	-10		10	%
VSYS SCP	VSYS_SCP		1.5	2	2.5	V
Input vs. battery voltage sleep threshold	Sleep_TH	VIN-VBAT start charging threshold	100	180	250	mV
	Sleep_TH_HYS	VIN-VBAT stop charging threshold	50	120	150	mV
Output VBAT and VDD characteristics						
Battery charge voltage regulation	CV	25tt，CV=4.2V	4.179	4.2	4.221	V
	CV	0°C to +50°C，CV=4.2V	4.168	4.20	4.232	V
Battery Over-Voltage Protection	VBAT_OVP	CV=4.2V	4.25	4.3	4.35	V
Constant Current Regulation	CC range	Register setting	8		512	mA
	CC Accuracy	VIN=5V, CC=200mA	186	200	214	mA
		VIN=5V, CC=96mA	89	96	103	mA
		VIN=5V, CC=48mA	44	48	52	mA
Trickle Threshold Voltage	$V_{PRE\_CHG\_TH}$	$V_{PRE\_CHG\_TH}$ =3V， VBAT	2.9	3	3.1	V

		rise				
Trickle Current Variation	I_{PRE_CH}	1/5 CC，CC=128mA	-10		10	%
Termination Charge Current	EOC Range		1		32	mA
	EOC Accuracy	EOC=1mA	0.8	1	1.2	mA
		EOC=3mA	2.7	3	3.3	mA
VDD Voltage Regulation	VDD	Load=10mA VDD=3V	2.9	3	3.1	V
VBAT quiescent current	I_{BAT_Q}	VDD disable, VBAT=4V, normal mode		2	3	uA
		VDD enable, VBAT=4V, normal mode		2.3	3.5	uA
	I_{BAT_Q}	LP mode，VBAT=4V		0.5	1	uA
VBAT leakage current in shipping mode	$I_{BAT\_SHIPPING}$	shipping mode,VBAT=4V		170	400	nA
BFET on resistance	$BFET\_R_{DSON}$	VIN=0V ， ISYS=0.5A, BAT=4V		130	180	mohm
Battery under-voltage lockout threshold	V_{BOFF}	VBAT fall，off BFET, V_{BOFF} =2.8V	2.7	2.8	2.9	V
	V_{BON}		2.9	3	3.1	V
VBAT leakage current (VBAT< V_{BOFF})	I_{BOFF}	VBAT=2V		1.7	2	uA
TC timer out	T.O_prech		50	60	70	Min
CC+CV timer out	T.O_normal	T.O_normal=5Hr	4	5	6	Hr
Recharge threshold voltage	Vre_ch	Vre_ch =0.2V	150	200	250	mV
BAT discharge current limit	I_{DIS_LIMIT}	I_{DIS_LIMIT} =2.2A	1.8	2.2	2.6	A
Reset by INT	T_{RST_DGL}	T_{RST_DGL} =16s	12	16	20	S
B-FET off lasting time by INT	T_{RST_DUR}	T_{RST_DUR} =4s	3	4	5	S
Exit shipping mode by INT	$T_{EXIT\_SHIPPING}$		1.5	2	2.5	S
STATUS, NTC,INT						
Maximum STATUS External load capability	I_{STATUS}			5		mA
INT assert time		Interrupt	110	125	140	uS
NTC voltage	$V_{NTC\_HOT\_TH}$	V_{NTC} fall， As a percentage of	32.5	34.5	36.5	%

		VIN,REG08<2:1>=00, NTC_HOT temperature =60℃				
	$V_{NTC\_HOT\_TH\_HSY}$	V_{NTC} rise，As a percentage of VIN, REG08<2:1>=00，NTC_HOT_HYS temperature =5℃		3.25		%
	$V_{NTC\_WT\_TH}$	V_{NTC} fall，As a percentage of VIN, NTC_WT temperature =45℃	42.7	44.7	46.7	%
	$V_{NTC\_WT\_TH\_HSY}$	V_{NTC} rise, As a percentage of VIN, NTC_WT_HYS temperature =5℃		3.75		%
	$V_{NTC\_COOL\_TH}$	V_{NTC} rise, As a percentage of VIN,,REG08<0>=0 , NTC_COOL temperature =10℃	66.25	68.25	70.25	%
	$V_{NTC\_COOL\_TH\_HSY}$	V_{NTC} fall, As a percentage of VIN, NTC_COOL_HYS temperature =5℃		3		%
	$V_{NTC\_COLD\_TH}$	V_{NTC} rise, As a percentage of VIN, NTC_COLD temperature =0℃	71.25	73.25	75.25	%
	$V_{NTC\_COLD\_TH\_HSY}$	V_{NTC} fall, As a percentage of VIN, NTC_COLD_HYS temperature =5℃		2.5		%
Thermal Protection						
Thermal shutdown threshold	T_{OTP}			150		℃
Thermal shutdown hysteresis	ΔT_{OTP}			25		℃
Die thermal loop threshold	Tdie	Tdie=120℃		120		℃

I²C Interface (SDA, SCL) (IP2333_I2C)						
Input low threshold level	V_{L_IN}	SCL/SDA	-	-	0.8	V
Input high threshold level	V_{H_IN}	SCL/SDA	1.6	-	-	V
Open drain output low threshold level	V_{L_OUT}	SDA,Sink 3mA current			0.2	V
Clock frequency	f_{SCL}	Standard mode	-	100	-	KHz
		Quick mode	-	400	-	KHz
START condition hold time	$t_{HD;STA}$	Standard mode	4	-	-	μs
		Quick mode	0.6	-	-	μs
Setup repeated START time	$t_{SU;STA}$	Standard mode	4.7	-	-	μs
		Quick mode	0.6	-	-	μs
Data hold time	$t_{HD;DAT}$	Standard mode	-	-	3.45	μs
		Quick mode	-	-	0.9	μs
Data setup time	$t_{SU;DAT}$	Standard mode	250	-	-	ns
		Quick mode	100	-	-	ns
Setup time STOP condition time	$t_{SU;STO}$	Standard mode	4	-	-	μs
		Quick mode	0.6	-	-	μs
Low period of the SCL Clock	t_{LOW}	Standard mode	4.7	-	-	μs
		Quick mode	1.3	-	-	μs
High period of the SCL Clock	t_{HIGH}	Standard mode	4	-	-	μs
		Quick mode	0.6	-	-	μs

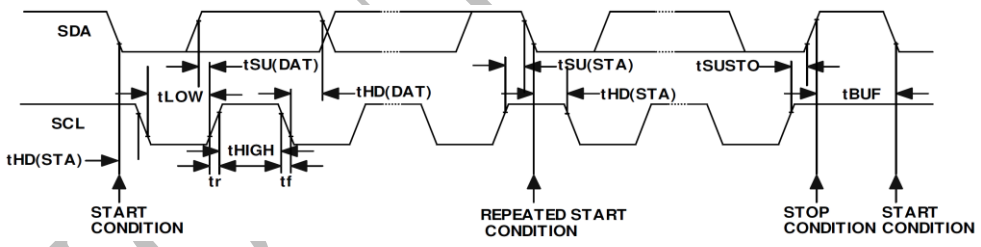


Fig3:IP2333_I2C I2C Timing

10. Detailed Description

BLOCK DIAGRAM

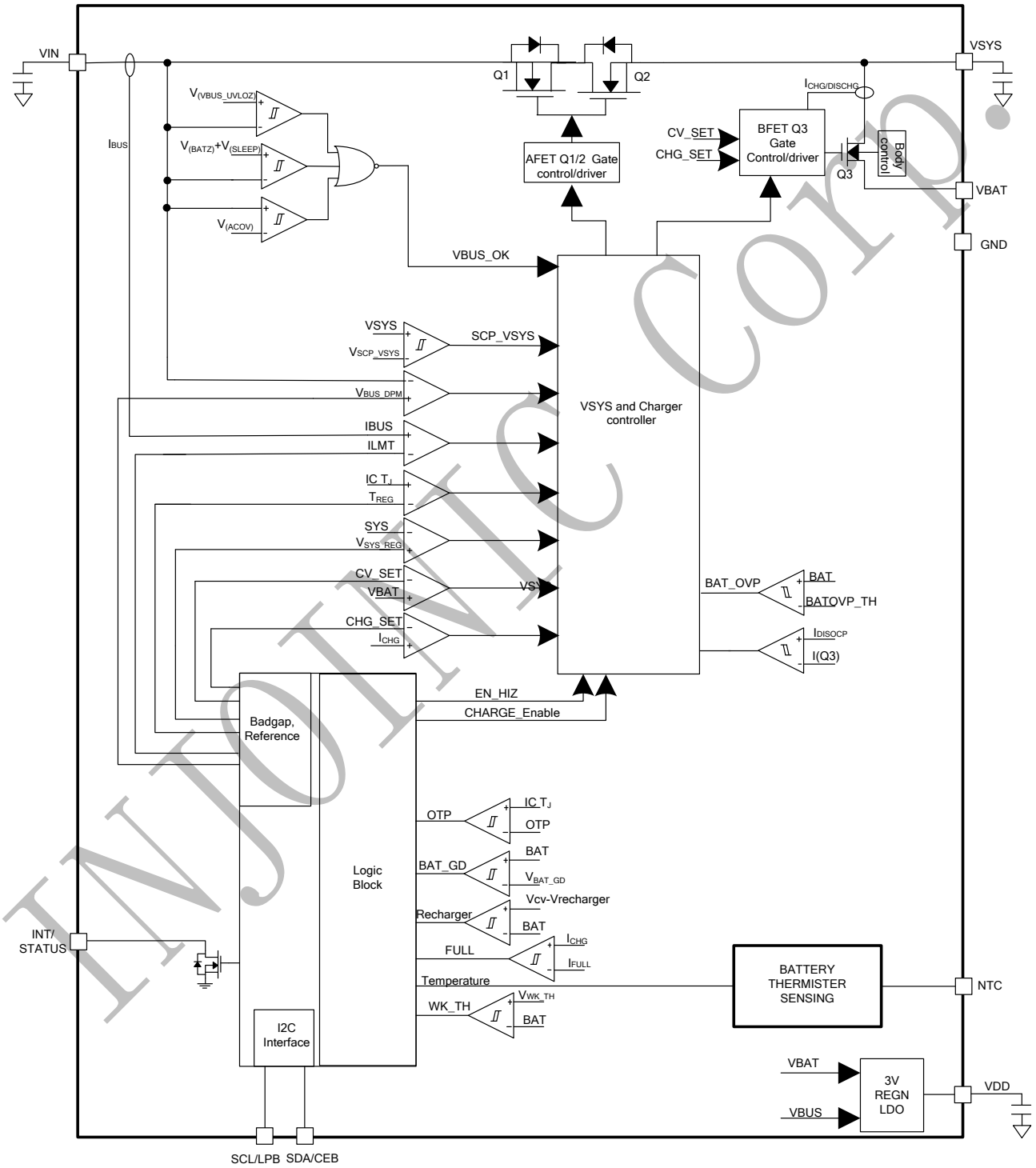


Fig 4: IP2333 Block

Overview

The IP2333 is an integrated I^{2}C-controlled (IP2333_I2C), single-cell Li-ion or Li-polymer battery charger with power path management function. The full-charge function includes constant current pre-charge, constant-current fast charge (CC) and constant voltage (CV) regulation, charge termination, auto-recharge, and a built-in safe charge timer. The power path function allows the input source to power the system and charge the battery simultaneously. The system load requirement always has priority to the charge current. When the input power is limited due to an input current limit or input voltage limit, the IC reduces the charge current automatically until the battery supplements the system load.

The IC integrates a LDO AFET between IN and SYS and a LDO battery BFET between SYS and BATT. In charging mode, battery FET works as a fully featured linear charger with pre-charge, fast constant current charge, constant voltage charge, charge termination, auto-recharge, NTC monitoring and JEITA standard charging, built-in safe timer out control, and thermal protection. The charge current can be programmed via the I^{2}C interface (IP2333_I2C). The IC adjusts the charge current when the die temperature exceeds the thermal regulation threshold (120°C default).

In supplement mode, the battery supplies to the system load simultaneously with battery FET ON when the input power is not sufficient enough to power the system load. When the input is removed, the battery FET is also fully turned on to allow the battery to power up the system.

When only the battery exists, IP2333 enters the low power consumption mode, I^{2}C enters the sleep mode, and the standby current is as low as 1uA in low power mode. It is very suitable for low lithium battery applications, such as smart wear, TWS etc.

Power Supply

The internal bias circuit of the IC is powered from the higher voltage of either VIN or BATT. When VIN rises above its under-voltage lockout (UVLO) threshold, all modules are all active, AFET LDO supply to system, If the battery voltage meets the charging conditions, BFET driver works and starts linear charging. The battery supplies to the system load simultaneously with BFET ON when the input power is not sufficient enough to power the system load. On shipping mode, BFET is OFF, battery detection comparator, I^{2}C interface are ready, the power consumption of the chip is less than 400nA.

I2C watchdog timer (IP2333_I2C)

Watchdog timer is invalid when VIN is ready and I^{2}C communication function is active at any time. When only the battery exists, watchdog timer is valid. If watchdog timer times out, I^{2}C communication module will enter standby mode in order to reduce power consumption. Master can wake up I2C function through falling edge of SCL. Once I^{2}C module is activated, IC can receive/send data again, and watchdog timer will work again. The I^{2}C watchdog timer value can be set through the register (REG05 [6:5]), or the watchdog timer function can be disable through the register (REG05 [7]).

Input VIN OVP, UVLO function

IP2333 input withstand voltage up to 23V. In order to ensure the normal function of the system and protect the battery, The IP2333 has an input over-voltage protection (OVP) threshold and input UVLO threshold. Once the input voltage is out of its normal range, the AFET (Q1,Q2) is turned off immediately. When the input voltage is identified as a good source, a 30ms deglitch time becomes active. If the input voltage is always normal among the

30ms deglitch time, the system starts up. Otherwise, Q1,Q2 remains off (see Fig 5, Fig 6).

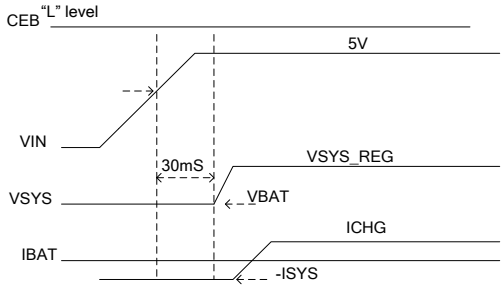


Fig5: VIN start

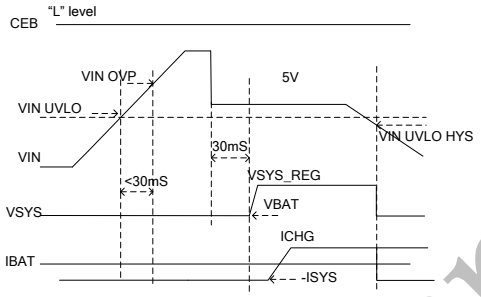


Fig6: VIN OVP and UVLO

AFET and BFET Power Path Management

The IC integrates a LDO AFET between VIN and SYS and a LDO battery BFET between SYS and BATT, AFET and BFET can bidirectional true shutdown for power path management function. The path management function can dynamic allocate power of the input adapter and priority to the power supply to the system to be compatible with all adapters and optimize the charging time. The path management function can also start up system with over discharged battery or no battery condition.

AFET turned off conditions：

- VIN>VIN OVP
- VIN<VIN UVLO
- REG01[4] AFET_ENB bit=1(IP2333_I2C)
- Within the system reset time by INT (IP2333_I2C)

BFET turned off conditions：

- Normal mode，VBAT<VBAT UVLO and VIN not OK
- VIN OK, REG01[3] CEB=1(IP2333_I2C) and not battery supplement mode
- VIN OK, CEB is high level and not battery supplement mode
- Shipping mode(IP2333_I2C)
- Within the system reset time by INT (IP2333_I2C)
- VIN OK, EOC function work with full charging battery
- VIN OK, NTC is out of range

System reset function by INT (IP2333_I2C)

IP2333_I2C INT pin can be used to cut off the path from VIN to VSYS and from VBAT to VSYS to reset the system manually if system application need. Once INT is pull low for longer than t_{RST_DGL} (which can be programmed by REG01 [7:5]), VSYS is disconnected from VIN by turning off AFET and from VBAT by turning off BFET. The off state lasts for t_{RST_DUR}, which can be programmed by REG01 [7:5]. Then the AFET and BFET are turned on automatically, and the system is powered again. The IP2333 can reset the system by controlling the INT pin (see Figure 7).

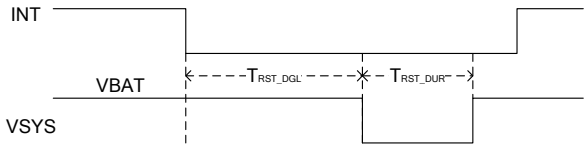


Fig7: System reset by INT

Input Dynamic Power Management (VIN-DPM and IIN-DPM)

To meet the input source's (typically USB) maximum current limit specification, the IP2333 uses an input current and voltage-based power management by monitoring the input current and voltage continuously. The input current and voltage limit can be programmed via the REG0[7:0] to prevent the input source from being over-loaded. Either the input current limit or the input voltage limit is reached, the Q1 and Q2 FET between VIN and VSYS are regulated so that the total input power is limited. As a result, the system voltage drops. Once the system declines to a minimum value of VSYS_REG - 135mV and VIN – 350mV, the charge current is reduced to prevent the system voltage from keeping dropping further. If the charging current drops to zero, but the system current continues to increase and the system voltage will continue to decrease. When the system voltage drops to meet the conditions of battery supply, the battery and adapter will supply power to the system together.

The voltage-based DPM regulates the input voltage to VIN_MIN, The current-based DPM regulates the input current to IIN_limit. In addition, IP2333 internally integrates sleep comparator, the IC can start to charge at VIN-VBAT>VIN_SLEEP_TH, so it is necessary to avoid triggering sleep comparator threshold, usually VIN-DPM is set to be greater than VBAT+ VIN_ SLEEP, The input voltage limit function can be disabled by REG07 [6].

VIN_MIN set via the I^2C should be at least 300mV higher than VBAT to ensure the stable operation of the regulator in any conditions.

Battery Charge Profile

The IP2333 provides three main charging phases: pre-charge, fast-current charge, and constant-voltage charge (see Figure 8). The IP2333 can safely pre-charge the deeply depleted battery until the battery voltage reaches the pre-charge to fast-charge threshold (VBATT_PRE). The pre-charge current is CC/5. If VBATT_PRE is not reached before the pre charge timer (1hr) expires, the charge cycle stops, and a corresponding timeout fault signal is asserted. When the battery voltage exceeds VBATT_PRE, the IP2333 enters a fast-charge phase. The fast-charge current can be programmed via register (REG02[5:0]). When the battery voltage rises to the battery-full voltage (CV) set via register (REG04[7:2]), the charge mode changes from CC mode to CV mode, and the charge current starts decreasing. When charge current decreases to EOC current set via I2C, the charger stop to charge and STATUS indicates end of charging. When the battery voltage is lower than the recharge threshold, the IC will automatically restart charging.

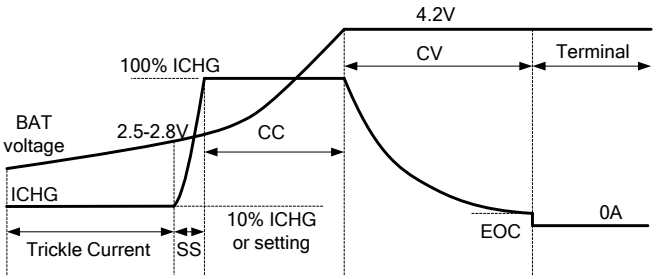


Fig8: Battery Charge Profile

Termination Charging (EOC) and Recharge

Assuming that the termination function is set via REG05[4] =1, battery voltage reach to CV，the charge cycle is considered to be completed when the ICHG is always smaller than EOC current and a 4ms delay. BFET is off and the charge status is updated to charge done. The termination charge current threshold (EOC) can be programmed via REG03[3:0].

With VIN-DPM，IIN-DPM and temperature loop, EOC function is masked. The charge current can also be terminated when the termination conditions are met if EOC set via REG05[4] =1. Otherwise, the charge current continues to taper off.

When the battery is fully charged and charging is terminated, the battery may be discharged due to system consumption or self-discharge. When the battery voltage is discharged below the recharge threshold and VIN is still in the operating range, the IP2333 begins another new charging cycle automatically. The auto-recharge function is valid only when the EOC function is ok.

VBAT OVP

The IP2333 is designed with a built-in battery over-voltage limit (about 100mV higher than VBATT_REG). When a battery over-voltage event occurs, the IP2333 suspends charging immediately and asserts a fault. The system resumes charging until the battery voltage drops below the recharge threshold.

VBAT UVLO

The IP2333 detects that the battery voltage is lower than the VBAT UVLO threshold, the battery discharge stop to prevent the deep discharge damage of the battery. When the battery voltage is higher than the VBAT UVLO threshold, the battery discharge function is restored. The VBAT UVLO threshold is set through register REG01 [2:0].

Battery Supplement mode

The charge current is reduced to keep the input current or input voltage in regulation when DPM occurs. If the charge current is reduced to zero and the input source is still overloaded due to a heavy system load, the system voltage begins decreasing. Once the system voltage drops to 25mV below the battery voltage, the IP2333 enters battery supplement mode, and the ideal diode mode is enabled. The battery FET is regulated to keep VBATT - VSYS at 25mV when I_{DSCHG} (supplement current) * R_{ON_BFET} is lower than 25mV. In the case that I_{DSCHG} * R_{ON_BFET} is higher than 25mV, the battery FET is fully turned on to maintain the ideal forward voltage. When the system load decreases, once VSYS is lower than VBATT + 20mV, the ideal diode mode is enabled.

In supplement mode, the EOC function is automatically turned off. If the system current decreases to VBAT = VSYS, the system exits supplement mode, as VSYS increases, and the charging current begins to increase. If input is invalid, BFET will be fully turned on to supply power to the system.

Thermal Regulation and Thermal Shutdown

The IP2333 monitors the internal junction temperature continuously to maximize power delivery and avoid overheating the chip. When the internal junction temperature reaches the preset limit of TJ_REG (120°C default), the IC starts to reduce the charge current to prevent higher power dissipation. The thermal regulation thresholds from 60 - 120°C can be set by I^2C to help the system design meet the thermal requirements in different applications. The junction temperature regulation threshold can be set via register (REG07[5:4]). When the junction temperature reaches 150°C, both Q1,Q2 and Q3 turn off. When the junction temperature decreases 25°C, the IC thermal shutdown releases.

Negative Temperature Coefficient (NTC) Temperature Sensor

NTC allows the IP2333 to sense the battery temperature using the thermistor (usually available in the battery pack) to ensure a safe operating environment for the battery and meet JEITA standard of charger. Connect appropriately valued resistors from VIN to NTC to ground. The resistor divider works with a thermistor connected from NTC to ground. The NTC voltage is determined by the resistor divider whose divide ratio depends on the temperature. The NTC function works only in charge mode. Once the NTC voltage is out of this divide ratio, the temperature is outside of the safe operating range and the IP2333 stops charging and report it on the status bits. Charging resumes automatically after the temperature falls back into the safe range.

For JEITA standard of charger, if V_{NTC} reached to the hot threshold $V_{NTC\_HOT\_TH}$ or cold temperature threshold $V_{NTC\_COLD\_TH}$ due to the battery temperature changing, the chip will turn off the charging function. When V_{NTC} reached to the warm or cool voltage range, charge voltage and charge current will decrease to set value that be set register (REG09 [3:0]).

The setting register can mask the NTC function. The IP2333 sets a pre-determined warm and cold bound of the divide ratio for NTC cold and NTC hot internally. Where $V_{NTC\_WT\_TH}$，$V_{NTC\_COLD\_TH}$ corresponding temperature of is 45 °C and 0 °C respectively, and the threshold values of cool and hot are set via register (REG08 [2:0]).

JEITA charging standard is shown in Figure 9:

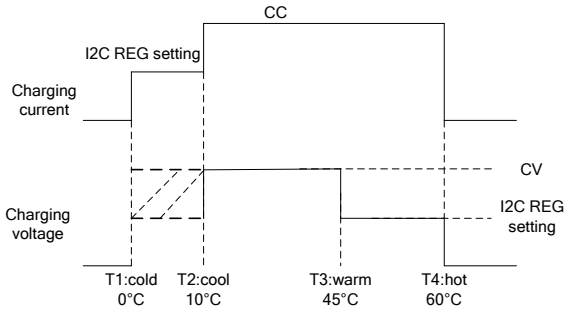


Fig9: JEITA Charging Standard

The figure below shown the NTC setting principle, selection the NTC resistance is NCP18XH103，B25/50=3380K, and the values of RT1 and RT2 can be determined by the following formula:

$$RT2 = \frac{V_{IN} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5}\right)}{RTH_{HOT} \times \left(\frac{V_{IN}}{VT5} - 1\right) - RTH_{COLD} \times \left(\frac{V_{IN}}{VT1} - 1\right)}$$

$$RT1 = \frac{\left(\frac{V_{IN}}{VT1} - 1\right)}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}}$$

If hot temperature is 60°C， so RTH_{COLD}= 27.22 kΩ， RTH_{HOT}= 3.01kΩ

VT1=73.25% x VIN， VT5=34.37% x VIN

so RT2=30.18kΩ, RT1=5.23kΩ

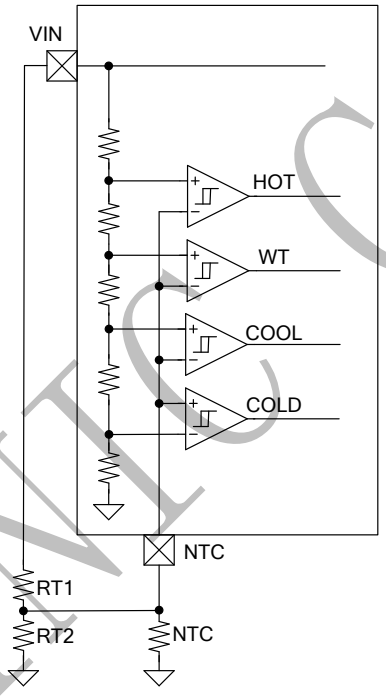


Fig10::NTC Setting

Safety Timer

The IP2333 provides both a pre-charge and fast-charge safety timer to prevent an extended charging cycle due to abnormal battery conditions. The safety timer is 60min when the battery voltage is lower than VBATT_PRE. The fast charge safety timer starts when the battery enters fast-charge mode. The fast-charge safety timer(3-24Hr) can be programmed through the REG05[2:1]. The safety timer can be disabled via the I^2C. The following actions can restart the safety timer:

A new charge cycle is kicked in.

- The input power is recycled
- REG01 [3] and CEB pin reset to charge enable
- Software and hardware reset system
- Write REG05 [3] from 0 to 1 (safety timer enable).
- System recharge.

Shipping mode(IP2333_I2C)

In applications where the battery is not removable, it is essential to disconnect the battery from the system for shipping mode or to allow the system power to be reset during the application. The IC has a register bit for battery disconnection control (BAT_FET_CTR). If this bit is set to 1, the IP2333 enters shipping mode after a delay time($T_{RST\_SHIPPING}$), which can be programmed by REG08[7:6]. The battery FET turns off and the BAT_FET_CTR bit refreshes to 0 after the battery FET turns off. In enter shipping mode, only BAT detection module and I2C communication module are active, The IC power consumption current is less than 0.5uA. If the shipping mode is set when INT is low, the system enters the shipping mode after INT becomes high.

To wake the IP2333 up from shipping mode:

- Plug in the input adapter.
- INT pin from high to low and continuously low for more than 2S.

VDD LDO

IP 2333 has a LDO output(VDD) with maximum 20mA load capacity. The output voltage is set through I^2C REG08 [5:4], and LDO output can be masked through register05[0]. VDD LDO does not output in shipping mode and low power consumption (LP) mode.

Charging State Indication

Charging status displays through status pin, including below status:

- Output low level(LED always on): Charging.
- Output high impedance: EOC, input over voltage and under voltage.
- 1Hz flashing: NTC over temperature / low temperature, charging timeout.

Low Power Mode

When the device is powered by the battery it is imperative that power consumption is minimized in order to maximize battery life. After system entre LP mode, IC standby power consumption is less than 1uA, all modules are invalid, and BFET is on. When VIN ok, system auto exit LP mode. LP mode function can be masked through setting REG02[7].

Interrupt to Host (INT)(IP2333_I2C)

The IP2333_I2C has an alert mechanism that can output an interrupt signal via INT to notify the system of the operation by outputting a 125μs low-state INT pulse. All of the below events can trigger an INT output:

- VIN OVP and VIN DPM
- VIN OK
- VBAT OVP
- EOC
- NTC cold and hot

When any fault occurs, the IP2333_I2C sends out an INT pulse and latches the fault state in fault status register. After the IP2333_I2C exits the fault state, the fault bit is reset to 0 after the host reads. The NTC fault bit is not latched and always reports the current thermistor conditions. The INT signal can be masked when the corresponding control bit is set in REG06[4:0]. When an INT condition is masked, this means that the INT pin

signal will not trigger when the corresponding condition occurs. Masking INTs is useful when writing software code to avoid unnecessary interruptions due to these events.

When any interrupt condition occurs, other interrupt triggers will be shielded. It is necessary to mask the interrupt condition through the corresponding register to remove the shielding of other interrupts.

Battery discharge OCP

If the battery is connected and the input source is missing, the battery FET is fully on when VBATT is above the VBATT_UVLO threshold, then battery FET minimizes conduction loss during discharge. The low R_{ds-on} resistance and low quiescent current help extend the running time of the battery. Battery discharge current exceeds the discharge current limit which be setting by register03 [6:4], the battery discharge over current protection works, turn off BFET after 60us and enters hiccup mode.

System SCP function

The IP2333 features VSYS short-circuit protection (SCP) for both the VIN to VSYS path and the VBAT to VSYS path. The system voltage is monitored continuously. If VSYS is lower than SCP threshold value after a 100μs delay, system SCP for both the VIN to VSYS path and the VBAT to VSYS path is active. Both AFET and BFET are turned off immediately, and the IP2333 enters hiccup mode. The system restart interval is 64ms the hiccup mode until SCP disappear.

VIN OK，SCP trigger condition：

- VSYS<2.4V
- SCP time>100uS

IP2333_I2C register MAP

Default Device Address: **23H（read）** and **22H（write）**.

MSB							LSB
0	0	1	0	0	0	1	R/W

INPUT Register, OFFSET=0x00, Default value=0x9F

Bit(s)	Name	Description	R/W	Reset
7:4	VIN_MIN<3:0>	VDPM Threshold Offset: 3.68V，80mV Step Range: 3.68V – 4.8 V(0001-1111) Default: 4.32V （1001）	RW	1001
3:0	ILMT_SET<3:0>	Input Current Limit Offset: 50mA，30mA Step Range: 50mA –500mA(0000-1111) Default: 500mA（1111）	RW	1111

MOSFETs setting register: Offset=0x01, Default value=0xA4

Bit(s)	Name	Description	R/W	Reset
7:5	TRST_DGL TRST_DUR	The low-level time by pulling down the INT pin for reset system（TRST_DGL） The system recover time by pulling down the INT pin for reset system（TRST_DUR） 000：TRST_DGL=8S、 TRST_DUR=2S 001：TRST_DGL=8S、 TRST_DUR=4S 010：TRST_DGL=12S、TRST_DUR=2S 100：TRST_DGL=16S、TRST_DUR=2S 101：TRST_DGL=16S、TRST_DUR=4S 110：TRST_DGL=20S、TRST_DUR=2S Default: TRST_DGL=16S、TRST_DUR=4S（101）	RW	101
4	AFET_ENB	AFET ON/OFF control 0: ON 1:OFF Default: ON（0）	RW	0
3	CEB	Charge Control 0:enable 1:disable Default: enable（0）	RW	0
2:0	VBAT_UVLO<2:0>	Battery UVLO Threshold offset:2.4V, 100mV Step Range: 2.4 V – 3.1 V(000-111) Default: 2.8 V （100）	RW	100

CC setting register: Offset=0x02, Default value=0x8F

Bit(s)	Name	Description	R/W	Reset
7	LPB_EN	LP Mode Control 0:enable 1:disable Default: disable（1）	RW	1
6	RSV	RSV	RW	0
5:0	CC<5:0>	Charge Current Offset: 8mA，8mA Step Range: 8mA –512mA(000000-111111) Default: 128mA（001111）	RW	001111

Current threshold setting register:Offset=0x03, Default value=0x71

Bit(s)	Name	Description	R/W	Reset
7	RSV	RSV	RW	**0**
6:4	IDSCHG<2:0>	Discharge Current 000：250mA;　001：500mA 010：750mA;　011：1050mA 100：1350mA;　101：1750mA 110：2200mA;　111：3100mA Default: 3100mA（111）	RW	111
3:0	EOC<3:0>	Termination Charge Current Offset: 1mA，2mA Step Range: 1mA –31mA(0000-1111) Default: 3mA（0001）	RW	0001

Charging setting register: Offset=0x04, Default value=0xA3

Bit(s)	Name	Description	R/W	Reset
7:2	CV<5:0>	Constant Voltage Offset: 3.6V，15mV Step Range: 3.6V –4.545V(000000-111111) Default: 4.2V（101000）	RW	101000
1	V_{WK_SET}	Pre-charge Voltage Threshold 0:2.8V 1:3V Default: 3V（1）	RW	1
0	RCHG_SET	Recharge Voltage Threshold 0:CV-100 mV, 1:CV-200 mV Default: 200mV（1）	RW	1

Control register1: Offset=0x05, Default value=0xBB

Bit(s)	Name	Description	R/W	Reset
7	EN_WTD	Watchdog Control 0:Disable 1:enable Default: enable（1）	RW	1
6:5	WTD<1:0>	Watchdog Timer 00:10s;　01:20s; 10:40s;　11:80s; Default: 20s（01）	RW	01
4	EN_EOC	EOC Control 0:Disable 1:enable Default: enable（1）	RW	1
3	TIMER_EN	Timer Control 0:Disable 1:enable Default: enable（1）	RW	1
2:1	CHG_TMR<1:0>	Timer 00:3hour;　01:5hour; 10:8hour;　11:12hour Default: 5hour（01）	RW	01
0	EN_LDO	VDD Control 0:disable 1:enable Default: enable（1）	RW	1

Control register2: Offset=0x06, Default value=0x80

Bit(s)	Name	Description	R/W	Reset
7	EN_NTC	NTC Control 0:Disable 1:Enable Default: enable（1）	RW	1
6	RSV	RSV	RW	0
5	BATFET_CTL	BFET Control 0: ON 1: OFF Default:ON（0）	RW	0
4	PG_INT_EN	PG_INT Control 0: Disable 1: Enable Default: Disable（0）	RW	0
3	EOC_INT_EN	EOC_INT Control 0: Disable 1: Enable Default: Disable（0）	RW	0
2	RSV	RSV	RW	0
1	NTC_INT_EN	NTC_INT Control 0: Disable 1: Enable Default: Disable（0）	RW	0
0	BATTOVP_INT_EN	BATTOVP_INT Control 0: Disable 1: Enable Default: Disable（0）	RW	0

Control setting register3: Offset=0x07, Default value=0X39

Bit(s)	Name	Description	R/W	Reset
7	PCB_OTP_EN	PCB_OTP Control 0: Disable 1: Enable Default: Disable（0）	RW	0
6	DPM_ENB	DPM Control 0:Enable 1: Disable Default: Enable（0）	RW	0
5:4	TJ_REG<1:0>	Junction Operating Temperature 00: 60°C 01: 80°C 10: 100°C 11: 120°C Default: 120°C（11）	RW	11
3：0	VSYS REG<3:0>	VSYS Voltage Offset: 4.2V，50mV Step Range: 4.2V –4.95(0000-1111) Default: 4.65V(1001)	RW	1001

Control setting register4: Offset=0x08, Default value=0x06

Bit(s)	Name	Description	R/W	Reset
7:6	SHP_DGL<1:0>	Enter shipping mode deglitch time 00: 1s 01: 2s 10: 4s 11: 8s Default: 1s（00）	RW	00
5:4	LDO_SET<1:0>	VDD Voltage 00:3V 01:2.5V 10:1.8V 11:1.5V Default: 3V（00）	RW	00
3	JEITA_CV_EN	CV setting control with cool temperature conditions according to JEITA standard 0:Disable 1:Enable Default: Disable（0）	RW	0
2:1	JEITA_HOT<1:0>	Hot temperature threshold 11:45°C: VNTC falling threshold:44.75% 10:50°C: VNTC falling threshold:41.25% 01:55°C: VNTC falling threshold:37.75% 00:60°C: VNTC falling threshold:34.5% Default: 45°C（11）	RW	11
0	JEITA_COOL	Cool temperature threshold 0：10°C， VNTC rising threshold:68.25% 1：15°C， VNTC rising threshold:65.25% Default: 10°C（0）	RW	0

Control setting register5: Offset=0x09, Default value=0x25

Bit(s)	Name	Description	R/W	Reset
7：5	I2C_SADDR	I2C device address 0010XXXY, XXX for default value	RW	001
4	RSV	RSV	RW	0
3:2	JEITA_CC<1:0>	CC setting with charging conditions according to JEITA standard 00: CC 01:1/2CC 10:1/4CC 11:1/8CC Default: 1/2CC（01）	RW	01
1:0	JEITA_CV<1:0>	CV setting with charging conditions according to JEITA standard 00: CV 01: CV-100mV 10:CV-200mV 11:CV-300mV Default: CV-100mV（01）	RW	01

Status register0: Offset=0x0D,

Bit(s)	Name	Description	R/W	Reset
7	WATCHDOG_FAULT	Watchdog fault 0: normal; 1: timer out trigger	R	

		Note: When fault occur, register has been read and cleared		
6:5	RSV	RSV	R	
4:3	CHG_STAT<1:0>	Charging status 00 – Not Charging, 01 –Wake up, 10 –CC+CV, 11 –FULL	R	
2	VIN_DPM	DPM status 0:Not DPM, 1:DPM	R	
1	RSV	RSV	R	
0	T_J REG	Junction temperature control 0: normal, 1:die junction thermal regulation status	R	

Status register1: Offset=0x0E,

Bit(s)	Name	Description	R/W	Reset
7:6	RSV	RSV	R	
5	VIN_FAULT	Input source status 0: Normal, 1: fault: OVP or bad source Note: When fault occur, register has been read and cleared	R	
4	THEM_SD	THEM status 0: normal 1:thermal shutdown Note: When fault occur, register has been read and cleared	R	
3	BAT_FAULT	Battery status 0: normal 1:battery OVP Note: When fault occur, register has been read and cleared	R	
2	TIME_OUT	Timer status 0: Normal, 1: timer expiration Note: When fault occur, register has been read and cleared	R	
1:0	NTC_FAULT<1:0>	NTC status 00:Normal 01:hot Fault 10:cold Fault 11:cool or warm fault	R	

11.Typical Application Schematic

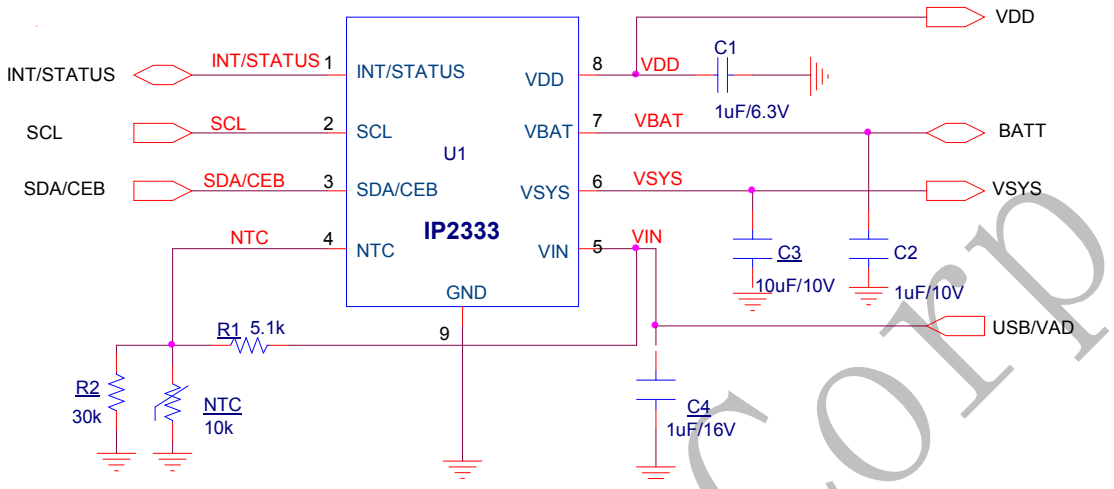


Fig11:IP2333 typical application schematic

12. Reference LAYOUT

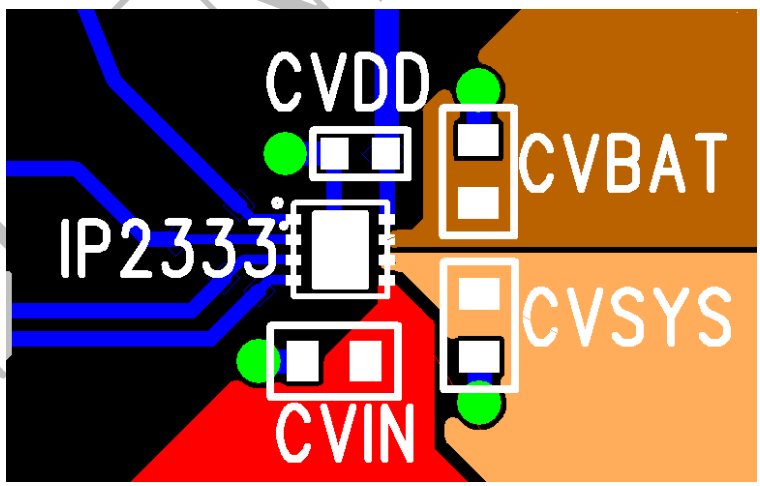
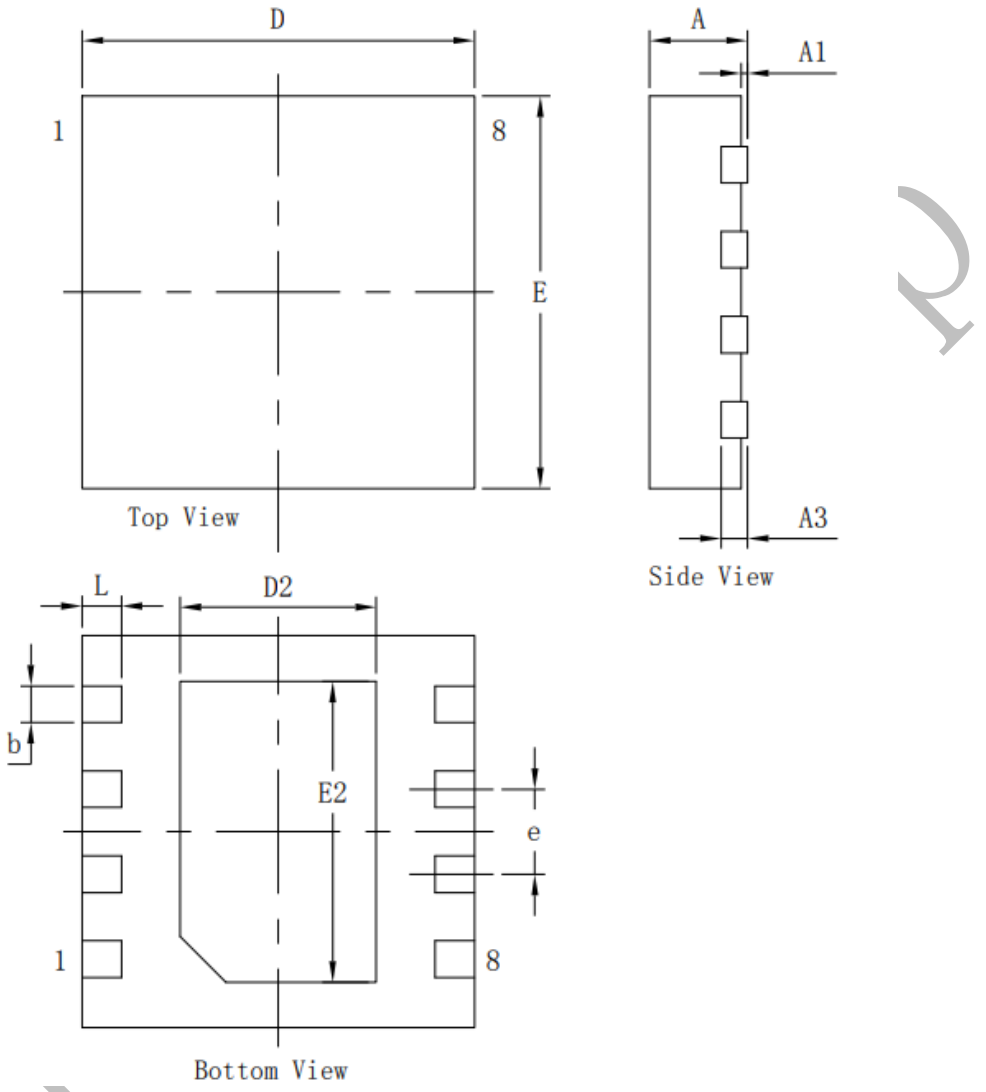


Fig 12: Layout Place out for key components

Note：CVIN, CVSYS, CVBAT, CVDD are close to IP2333 IC pins.

13. Package Information



SIZE / SYMBOL	MIN(mm)	Normal(mm)	MAX(mm)	SIZE / SYMBOL	MIN(mm)	Normal(mm)	MAX(mm)
A	0.70	0.75	0.80	E	2.90	3.00	3.10
A1	-	-	0.05	D2	1.40	1.50	1.60
A3	0.203 REF			E2	2.20	2.30	2.40
b	0.23	0.28	0.33	e	0.65 TYP		
D	2.90	3.00	3.10	L	0.25	0.30	0.35

Fig 13 IP2333 DFN8(0303) package sizes

14.IC Mark Description

Fig 14 IP2333 IC Mark Description

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