Apply To Multi-core Processor Full Integrated Smart Power Management Unit Top Specification

Features

- **Three synchronous step-down DCDC converters, can work in PSM (Pulse Skip Mode) and PWM mode, support dynamic voltage scaling operation(DVS).**
  - 2×DCDC Buck Converter(0.6V-3.6V, Up to 1A)
  - 1×DCDC Buck Converter(0.6V-3.6V, Up to 500mA)
- **Eight LDO Regulators**
  - 1×low-noise LDO(0.7V-3.4V, Up to 400mA)
  - 1×low-noise LDO(0.7V-3.4V, Up to 200mA)
  - 2×General LDO(0.7V-3.4V, Up to 200mA)
  - 2×General LDO(0.7V-3.4V, Up to 100mA)
  - 1×Mode-optional LDO(0.7V-3.4V, Up to 30mA)
  - 1×General LDO for internal use(3V, Up to 50mA)
- **Power Path**
  - Integrated Power Path management function simultaneously and independently powers the system and charges the battery
  - Support BAT terminal low battery(VIN>VBAT OK) insertion to wake-up function
- **Charger**
  - Supports up to 1A charge current
  - 25-mA minimum charge current
  - Programmable charge current with current monitoring output(ISET)
- **Programmable Function**
  - Power-up sequence and voltage can be programmed
  - Power-down sequence can be programmed
  - Abundant interrupt and wake-up function
- **Support external ON/OFF KEY**
  - Support Short-time /long-time key press interrupt and wake-up, which can be disabled
  - Support super long-time key press and RESET key press for reset function
- **Abundant Programmable Multi-function GPIOs**
- **Protection**
  - Support Under-Voltage Protection(UVP)
  - Support Over-Voltage Protection(OVP)
  - Support Over-Current Protection(OCP)
  - Support Over-Temperature Protection(OTP)
  - NTC protection for battery
- **Low Power Consumption**
  - 30 μA
- **Application Processor Interface**
  - I2C @200KHz MAX
  - POR(Power OK for Reset)
  - Interrupt Programmable
- **Package**
  - QFN32(0404)

Description

The IP6303 is an integrated power management IC which is full-integration, high efficiency and cost effective. It can be dedicated to multi-core processor application.

The device includes three programmable synchronous step-down DCDC converters which has 12.5mV minimum step, 2.0MHz highest switching frequency , up to 95% operation efficiency and 1.5A maximum load capacity. It can provide abundant stable energy for multiple processors, memorizers, peripheral equipment and other linear regulators. Base on the mission requirement the processor can control the voltage through I2C interface (DVS) for optimum power savings. In addition, the device contains eight LDO regulators. Six of the LDOs have their own input pin and programmable output voltage function. One normally enable LDO provides power for inner circuit.

Not only the default power-up and power-down sequence but also the default power voltage of all the power source can be programmed.

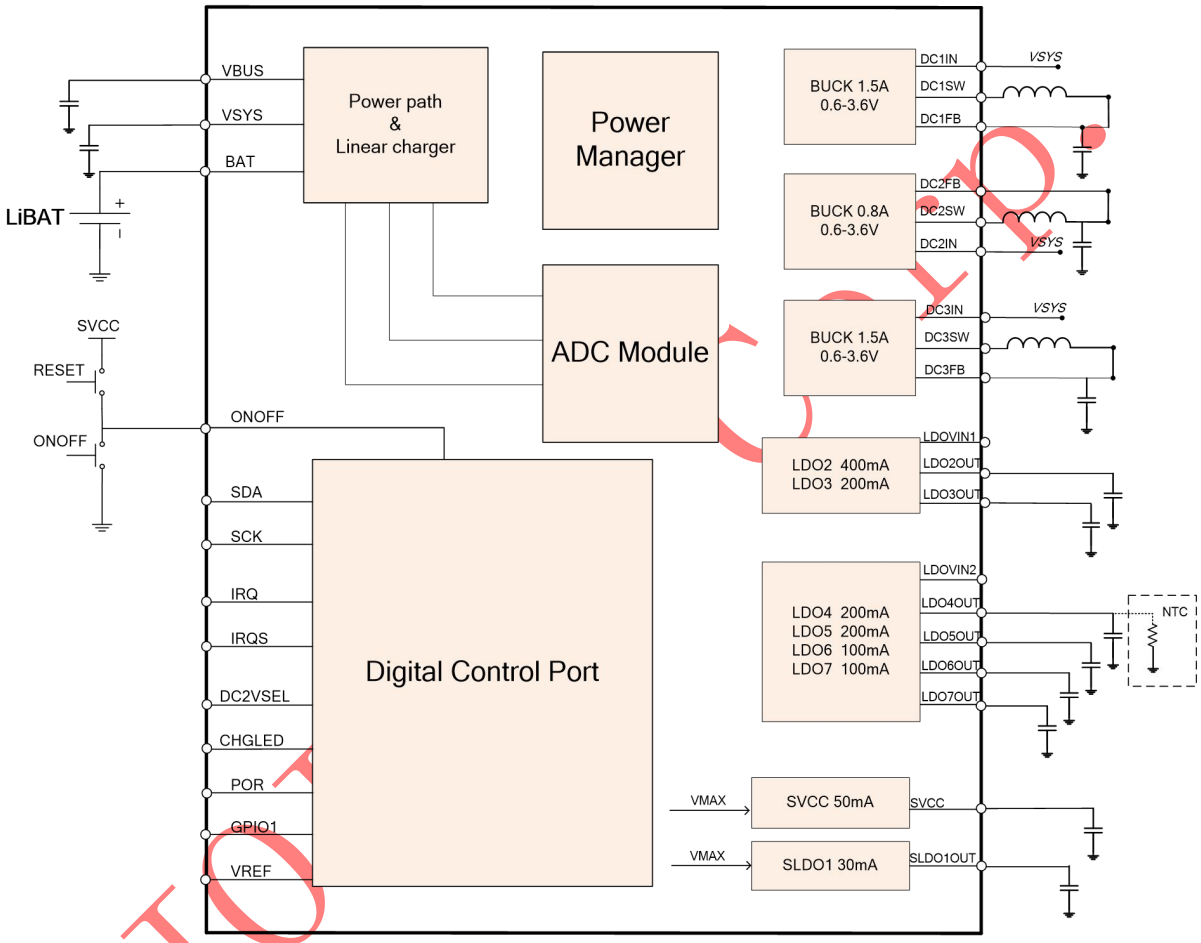
The IP6303 provide up to 1A charger current and as low as 25mA for Small capacity battery. In addition, the device integrates High precision ADC.

The IP6303 provide various kinds of interrupts and wake-up function. It also provides necessary protections, such as Under-Voltage Protection (UVP), Over-Voltage Protection (OVP), Over-Current Protection (OCP), Over-Temperature Protection (OTP).

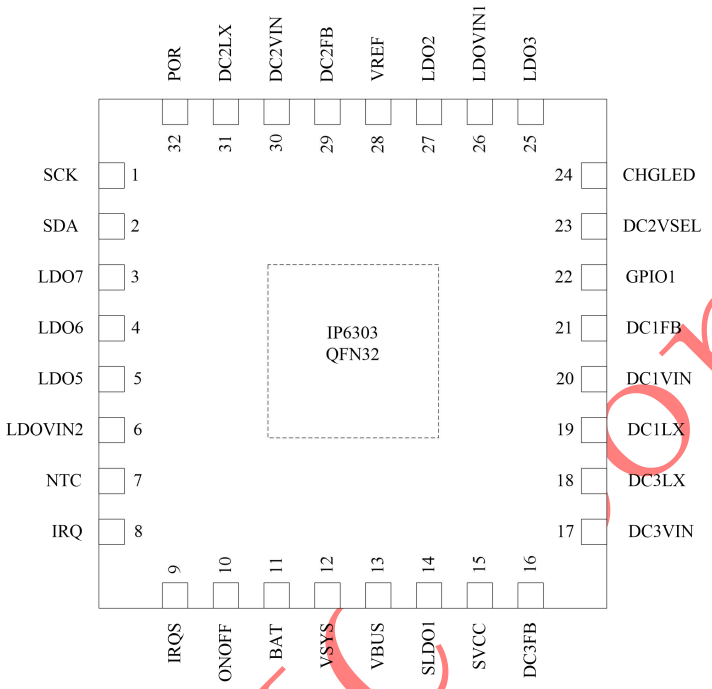
Applications

- **Smart Home**
  - Set Top Box(STB), the network broadcast box
  - Smart TV, Intelligent routers
- **Security and protection monitoring**
  - Car recorder, sport DV
- **Portable devices**
  - Tablet PC, E-book, navigator

Typical Application



Pin Description



Pin name	Pin number	Pin description
SCK	1	Clock pin for I2C serial interface, normally it connect a 2.2K resistor to 3.3V I/O power
SDA	2	Data pin for I2C serial interface, normally it connect a 2.2K resistor to 3.3V I/O power
LDO7	3	Output Pin of LDO7
LDO6	4	Output Pin of LDO6
LDO5	5	Output Pin of LDO5
LDOVIN2	6	LDO 4/5/6/7 input source
NTC	7	NTC Pin
IRQ	8	IRQ output
IRQS	9	IRQ wake-up signal input
ONOFF	10	ONOFF button input
BAT	11	Low voltage power input source（Li-Battery etc.）
VSYS	12	Power Path output
VBUS	13	High voltage power input source（5V Adapter etc.）
SLDO1	14	Output Pin of SLDO1
SVCC	15	Output Pin of SVCC

DC3FB	16	DCDC3 feedback pin
DC3VIN	17	DCDC3 input source
DC3LX	18	DCDC3 switch output
DC1LX	19	DCDC1 switch output
DC1VIN	20	DCDC1 input source
DC1FB	21	DCDC1 feedback pin
GPIO1	22	GPIO1
DC2VSEL	23	DCDC2 voltage select pin
CHGLED	24	Charger LED control pin
LDO3	25	Output Pin of LDO3
LDOVIN1	26	LDO 2/3 input source
LDO2	27	Output Pin of LDO2
VREF	28	Output Pin of Referance voltage
DC2FB	29	DCDC2 feedback pin
DC2VIN	30	DCDC2 input source
DC2LX	31	DCDC2 switch output
POR	32	Power good indication output

Absolute Maximum Ratings

PARAMETER	Value	UNITS
Voltage range on pins: VBUS, SYS, LDOVIN1 , LDOVIN2 , DC1VIN, DC2VIN, DC3VIN	-0.3 ~ 6	V
Operating Temperature Range , T_A	-40 ~ 85	℃
Junction Temperature Range, T_J	-40 ~ 150	℃
Storage temperature after soldering	-60 ~ 150	℃
Junction-to-ambient Thermal Resistance θJA	30	℃/W
Maximum ESD stress voltage， Human Body Model	>4K	V

Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{sleep}: SLEEP Mode Current	Deep-Sleep state		30		μA
V_{IL}: Logic Low Input Voltage				0.7	V
V_{IH}: Logic High Input Voltage		1.2			V

I2C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ADDRESS	Default		0x60		
f_{SCK}: Clock Operating Frequency			100	200	KHz

8-bit ADC

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Range of Channels	V_{BAT}	0.5		4.5	V
	I_{CHG}	0		1000	mA
	I_{BAT}	0		3000	mA
	V_{GP1}、V_{GP2}	-0.5		3.5	V
f_{ADC}			500		KHz

Power Path

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
BAT→VSYS			100		mΩ
VBUS→VSYS			160		mΩ

Charger

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CHGIN}: Input voltage		3		5.5	V
I_{CHG}		25		1000	mA
V_{CHG}	CGENDV = 11		4.40		V
	CGENDV = 10		4.35		
	CGENDV = 01		4.30		
	CGENDV = 00		4.20		

DCDC1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}: Input voltage		3		5.5	V
V_{OUT}: Output voltage	Vset = 0000_0000		0.6		V
	Vset = 0010_0000		1.0		
	Vset = 1111_0000		3.6		
	PSM Mode	-5		+5	%
	PWM Mode	-2		+2	%
$V_{OUTSTEP}$: Output voltage step			12.5		mV
I_{OUTmax}: Rated output current			1500		mA
I_{LIM}: PMOS current limit			2500		mA

Output voltage transition rate	R_STEP = 11 R_STEP = 10 R_STEP = 01 R_STEP = 00		0.78 3.1 6.25 12.5		mV/μs
$R_{DS(ON)\_PMOS}$: P-channel MOSFET On-resistance			125		mΩ
$R_{DS(ON)\_NMOS}$: N-channel MOSFET On-resistance			100		mΩ
f_{OSC}: Switching frequency	DC_FRQ[2:0] = 011		1.2		M
Duty cycle				100	%
R_{DIS}: Discharge resistor for power-down sequence			100		Ω

DCDC2

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}: Input voltage		3		5.5	V
V_{OUT}: Output voltage	Vset = 0000_0000 Vset = 0010_0000 Vset = 1111_0000		0.6 1.0 3.6		V
	PSM Mode	-5		+5	%
	PWM Mode	-2		+2	%
$V_{OUTSTEP}$: Output voltage step			12.5		mV
I_{OUTmax}: Rated output current			800		mA
I_{LIM}: PMOS current limit			2500		mA
Output voltage transition rate	R_STEP = 11 R_STEP = 10 R_STEP = 01 R_STEP = 00		0.78 3.1 6.25 12.5		mV/μs
$R_{DS(ON)\_PMOS}$: P-channel MOSFET On-resistance			380		mΩ
$R_{DS(ON)\_NMOS}$: N-channel MOSFET On-resistance			265		mΩ
f_{OSC}: Switching frequency	DC_FRQ[1:0] = 10		1.2		MHz
Duty cycle				100	%
R_{DIS}: Discharge resistor for power-down sequence			100		Ω

DCDC3

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}: Input voltage		3		5.5	V
V_{OUT}: Output voltage	Vset = 0000_0000 Vset = 0010_0000 Vset = 1111_0000	-2%	0.6 1.0 3.6	2%	V
	PSM Mode	-5		+5	%
	PWM Mode	-2		+2	%

$V_{OUTSTEP}$: Output voltage step			12.5		mV
I_{OUTmax}: Rated output current			1500		mA
I_{LIM}: PMOS current limit			2500		mA
Output voltage transition rate	R_STEP = 11 R_STEP = 10 R_STEP = 01 R_STEP = 00		0.78 3.1 6.25 12.5		mV/μs
$R_{DS(ON)\_PMOS}$: P-channel MOSFET On-resistance			110		mΩ
$R_{DS(ON)\_NMOS}$: N-channel MOSFET On-resistance			110		mΩ
f_{OSC}: Switching frequency	DC_FRQ[1:0] = 10		1.2		MHz
Duty cycle				100	%
R_{DIS}: Discharge resistor for power-down sequence			100		Ω

SVCC

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}: Input voltage	VSYS	3		5.5	V
V_{OUT}: Output voltage		2.6		3.3	V
$V_{OUTSTEP}$: Output voltage step			100		mV
I_{OUTmax}: Rated output current			50		mA
$R_{DS(ON)}$: MOSFET On-resistance					mΩ
R_{DIS}: Discharge resistor for power-down sequence			100		Ω
R_{OUT}: VOUT internal resistance			200		kΩ
Output Noise,<20KHz			100		μV_{RMS}

SLDO1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}: Input voltage	VSYS	3		5.5	V
V_{OUT}: Output voltage		0.7		3.4	V
$V_{OUTSTEP}$: Output voltage step			100		mV
I_{OUTmax}: Rated output current			30		mA
$R_{DS(ON)}$: MOSFET On-resistance					mΩ
R_{DIS}: Discharge resistor for power-down sequence			100		Ω
R_{OUT}: VOUT internal resistance			200		kΩ
Output Noise,<20KHz			100		μV_{RMS}

LDO2~3

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}: Input voltage	LDOIN1	3		5.5	V
V_{OUT}: Output voltage		0.7		3.4	V
$V_{OUTSTEP}$: Output voltage step			25		mV

I_{OUTmax}: Rated output current	LDO2		400		mA
	LDO3		200		mA
$R_{DS(ON)}$: MOSFET On-resistance					mΩ
R_{DIS}: Discharge resistor for power-down sequence			100		Ω
R_{OUT}: VOUT internal resistance			200		kΩ
Output Noise,<20KHz			30		μV_{RMS}

LDO4~7

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}: Input voltage	LDOIN2	3		5.5	V
V_{OUT}: Output voltage		0.7		3.4	V
$V_{OUTSTEP}$: Output voltage step			25		mV
I_{OUTmax}: Rated output current	LDO4、LDO5		200		mA
	LDO6、LDO7		100		mA
$R_{DS(ON)}$: MOSFET On-resistance					mΩ
R_{DIS}: Discharge resistor for power-down sequence			100		Ω
R_{OUT}: VOUT internal resistance			200		kΩ
Output Noise,<20KHz			30		μV_{RMS}

32-kHz RTC CLOCK

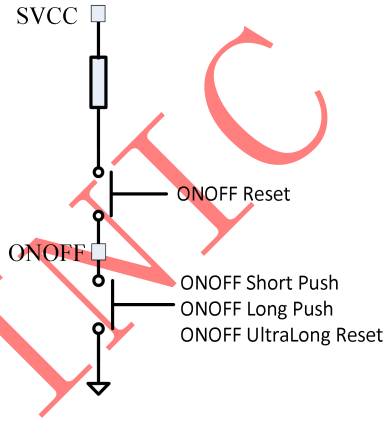
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output duty cycle		40	50	60	%
	built-in RC oscillator				
Crystal frequency			32.768		kHz
Crystal load capacitor			15		pF
Oscillator startup time			200		ms
Ground current					μA
	built-in RC oscillator				
Crystal frequency		-10%	32.768	+10%	kHz
Frequency accuracy	@ 25°C	-10		+10	%
Settling time				100	μs
Ground current					μA

Detailed Description

Power Reference

IP6303 has internal reference voltage, the filter capacitors must be connected between the VREF pin and the GND.

ONOFF Key



ONOFF functions as below:

- ONOFF Reset: When the ONOFF Reset key is pressed for more than 60ms, a reset signal will be issued. And all outputs except SVCC will be powered off, including SLDO1, which is in S3 state. After the ONOFF Reset key is released, the outputs will be powered on to S1 state.
- ONOFF Ultra-Long Reset: When the duration from pressing to releasing the button exceeds 8s, a reset signal will be issued. And the reset processing method is completely the same as ONOFF Reset.
  The ONOFF Reset and ONOFF Ultra Long Reset functions can be disabled by the register.
- ONOFF Short Push: When the duration of the ONOFF key from pressing to releasing is within the range of 60ms~1s (configurable time), an ONOFF Short Push event will be issued.
- ONOFF Long Push: When the ONOFF key is pressed for more than 1s, an ONOFF Long Push event will be issued.

ONOFF Short Push and ONOFF Long Push will not occur simultaneously in one key press. ONOFF Short Push and ONOFF Ultra-Long Reset will not occur simultaneously in one key press. ONOFF Long Push and ONOFF Ultra Long Reset may occur simultaneously in one key press. After ONOFF Long Push occurs, as long as the ONOFF key is not released, the timer will continue to count and issue a reset signal after 8s.

In S2 and S3 state, as long as the corresponding wake-up function is enabled, both ONOFF Short Push and ONOFF Long Push can wake up the system. When the chip is first powered on, the system can only be

awakened by ONOFF Short Push.

In S1 state, both ONOFF Short Push and ONOFF Long Push can generate interrupt events.

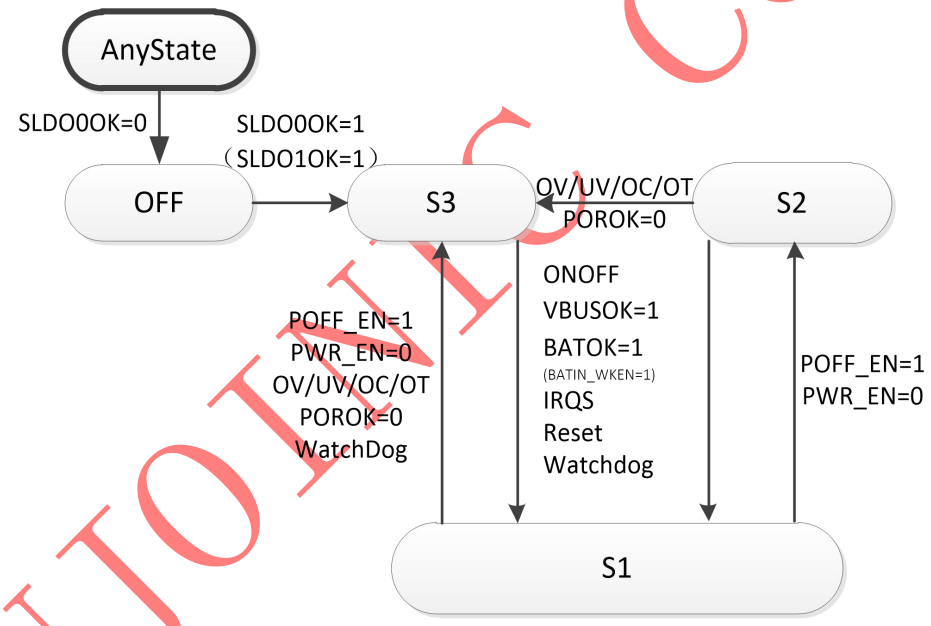
State-Machine

• **NO SUPPLY**: The system voltage is not high enough to power the SVCC regulator to maintain the device's operation. A global reset is asserted in this case. Everything on the device is OFF.

• **SLEEP MODE（S3）**: Device's POWER-OK (POR) signal is low, I2C communication is inactive. Power Path has been shut down. All the power supplies are OFF except the SVCC regulator and SLDO1 (if *LDO1_ALYON*=1).

• **STANDBY MODE（S2）**: Device's POWER-OK (POR) signal is low, I2C communication is inactive. All the power supplies are determined by the registers which had been set while the device was active.

• **ACTIVE MODE（S1）**: Device POWER OK (POR) signal is high, I2C communication is active. All the power supplies and IO can be controlled by the software.



Device POWER ON enable condition：

1、 If the ON/OFF key wake-up function is set and the pre-set key wake-up conditions are met when the device is in the SLEEP state, IP6303 can be POWER-ON enabled.

2、 If the VBUS_OK wake-up function is set and the VBUS voltage rising above the VBUS wake-up threshold(depending on the register setting), IP6303 will POWER ON automatically.

3、 If the VBAT_OK wake-up function is set and the VBAT voltage rising above the VBAT wake-up threshold(depending on the register setting), IP6303 will POWER ON automatically.

4、 If the external interrupt wake-up function is set and the interrupt trigger condition occurs when the device is in the SLEEP state, IP6303 can be POWER-ON enabled.

5、 In the ACTIVE state, if the WDOG_EN bit is set and the WDOG_CLR bit is not be clear in time, the IP6303 will POWER OFF immediately and POWER ON automatically after 2 seconds.

Device SLEEP MODE enable conditions：

1、 In the ACTIVE state, POFF_EN bit is set to 1.

2、 When the abnormal situation occur and trigger the smart protect functions, IP6303 will POWER OFF automatically. By reading the related registers can inquire the cause of POWER-OFF.

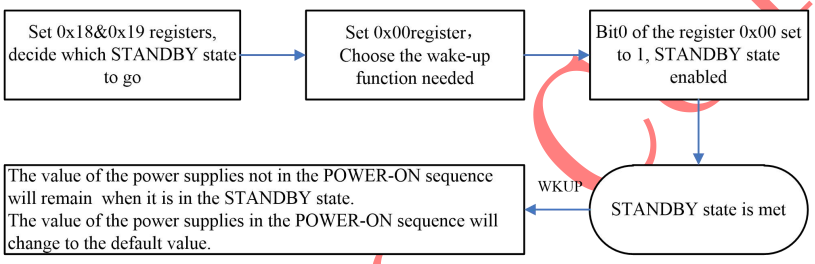
Device STANDBY MODE enable conditions：

If any of the LDOx_KEEPON bit or DCDCx_KEEPON bit is set, IP6303 will turn into STANDBY MODE after POFF_EN bit is set.

Device reset scenarios：

1、 When all of the power supplies of the device is OFF, all the information of IP6303 is reset.

2、 If the ON/OFF reset functions (super long-time key reset or single-key reset) is set and the pressing time get to the pre-set key time, IP6303 will reset immediately until the key was lifted. In this case all the information but RTC will be reset.

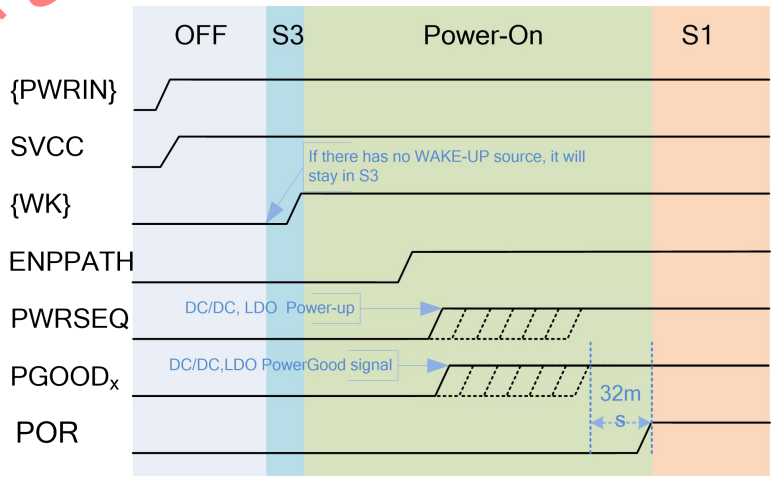


Power-on/off Schedule

The power-up sequence and the time slot for DCDC1~3、LDO1~7can be set according to the applications.

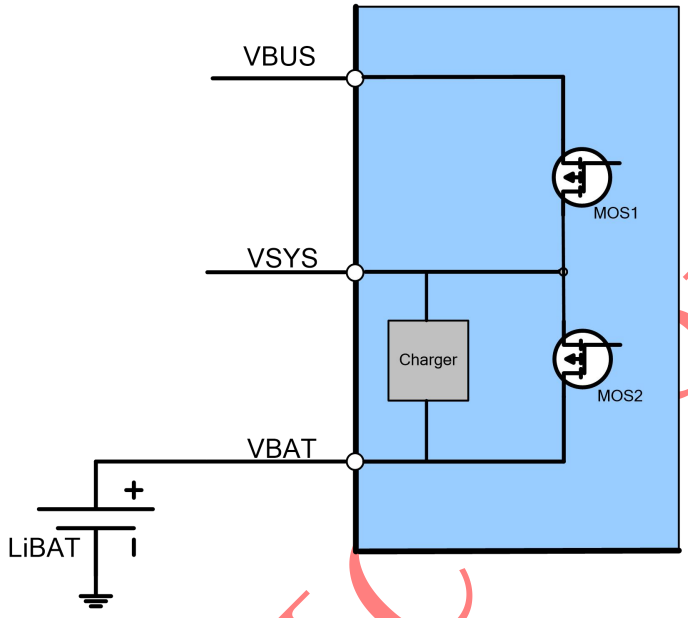
There are 7 optional steps in the power-up sequence, and the selectable time interval between each step is 1/2/4/8 ms. Each one of the Step-Down Converters and LDO Regulators can be factory programmed into any steps. After all the enabled power supplies are powered up, the POWER-OK signal (POR) will be set in 16/32 ms.

There are two options for POWER-OFF schedule. One is all the power supplies turn to OFF at the same time, the other is the POWER-OFF sequence is contrary to the sequence of POWER-ON and also has the same time slot.



Power Path

As shown in Figure below, VSYS is the common power source for all the power supplies, including Step-Down Converters, LDO Regulators and Charger. VBUS is recommended as HIGH Voltage input, such as 5V ADAPTER and USB interface. VBAT is recommended as LOW Voltage input, such as Li-battery.



Power Resources

IP6303 contains three Step-Down Converters (DCDCs) and LDO Regulators (LDOs).

POWER SUPPLY	VOLTAGE (V)	PRECISION (mV)	CAPACITY (mA)	Noise(uV)
DCDC1	0.6...3.5	12.5	1000	
DCDC2	0.6...3.5	12.5	500	
DCDC3	0.6...3.5	12.5	1000	
SLDO1	0.7...3.4	100	30	
LDO2	0.7...3.4	25	400	30
LDO3	0.7...3.4	25	200	30
LDO4	0.7...3.4	25	200	
LDO5	0.7...3.4	25	200	
LDO6	0.7...3.4	25	100	
LDO7	0.7...3.4	25	100	
SVCC	2.6...3.3	100	50	

The POWER ON/OFF sequence and default voltage of DCDC1~3 and LDO1~7 can be programmed according to the requirement.

In the ACTIVE state, the main processor can both enable and disable any one of the power supplies by rewrite the value of the relevant register. Otherwise, it can also modify the output voltage of all the power supplies within the effective range.

Before leaving the ACTIVE state, the main processor can decide which power supply would be maintained or disable in STANDBY state by rewriting the registers (REG: 0x18&0x19). At the same time, the power-off sequence and time slot can also be changed.

DCDC

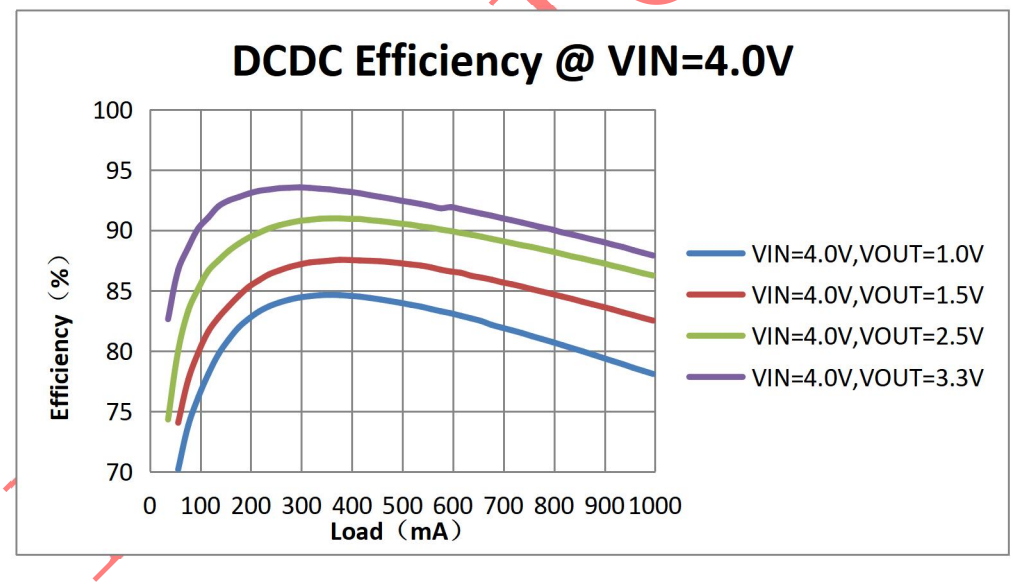
The switching frequency of DCDCs can range up to 2.0MHz. Designed by the method of four phases staggered, thanks to the spread-spectrum function, the DCDCs can greatly reduce the EMI problems.

When regulating the output voltage, the voltage changing rate can be set in order to reduce the inrush current caused by the leap voltage.

About DCDC2, except for the pre-set voltage, there are other two voltage can be set by the state of DC2VSEL pin in order to support different kinds of DRAM in different applications. The setting ways are list below:

DC2VSEL connects to SVCC	DC2VSEL connects to GND	DC2VSEL floating
Configuration	1.35V	1.5V

DCDC Typical Efficiency



LDO

LDO2 and LDO3 are low-noise linear regulators. These two LDOs mainly applied to the modules which have highly requirement to the noise, such as Audio、WIFI、Bluetooth、PLL. The other LDOs are general linear regulators.

SVCC, the default voltage is 3.0V, is mainly supply for the internal logic and IO. Its voltage can be modified in the first time working in ACTIVE state. As long as the supply of the system is not completely off, it can maintain the adjusted voltage value.

Except for SVCC, any LDOs can be set to SWITCH mode.

Linear Charger

IP6303 integrates a linear charger with a maximum charging current of 1A. The constant charge current can be modified form 25mA to 1.0A by I2C interface in ACTIVE MODE. In applications without I2C interface, the charging current can also be set by means of an ISET pin.

When the battery voltage is lower than 3V, the trickle charge current is adaptive to 0.1 times of the constant current. When the battery voltage is higher than 3V, the constant charge current will rise to the preset value in REGISTER 0x53. When the battery voltage is near the preset battery voltage, it will enters constant voltage charging stage. When the charging current is less than 100mA (REG 0X51)and battery voltage is near the constant voltage charging stage, the charging process is stopped. When the charging stage is accomplished, once the battery voltage falls under 4.1V, battery charging stage will be restarted.

When the VIN voltage is higher than 3.8V, and the VIN voltage is higher than VBAT+100mV, and VIOK=1, the charger will be allowed to turn on. The constant current charging current of IP6303 charger gradually increases. When entering CC mode, the charging current is adjusted every 0.128s (can be set by register).

IP6303 charger can automatically monitor IC temperature. When the IC temperature is above 100 degrees Celsius, the IC will reduce the charging current by one gear and detect the IC temperature again. If the IC temperature is still above 100 degrees Celsius, the current gear will be further reduced until the IC temperature is below 95 degrees Celsius (5 degrees Celsius hysteresis), and the charging will remain at the current current gear. If the IC temperature is below 80 degrees Celsius, the IC will increase the current gear until the current reaches the set charging current level. If the temperature exceeds 125 degrees Celsius, the IC will directly set the charging current to the minimum gear and turn off CHGOP.

IP6303 can also detect the temperature of the battery by connecting the negative temperature coefficient resistor (NTC) network outside the chip. Attach the NTC resistor to the battery or other location closest to the battery. And when the temperature is detected within the range of 0-45 degrees Celsius, the IC is in a normal charging state. When the temperature is detected to be above 45 degrees Celsius, the charging current is reduced by half(whether the function can be enabled through register configuration). When the temperature is detected to be above 55 degrees Celsius, the IC stops charging.*You can find more NTC detail information in NTC specification.*

The actual charging current is affected by the VBUS voltage. When the VBUS voltage is too low and below the set undervoltage value, IP6303 will automatically reduce the charging current to maintain the stability of the VBUS voltage. When the VBUS voltage drops below VBAT+40mV, the charging current will decrease to the minimum gear, and the IC will turn off charging.

The software operation process is as follows:

1. Before the software enables the charging function, the IC needs to first detect the presence of a

battery: First, set ENBATDT to 1. Wait for DTOVER to become 1. And then check the value of BATEXT (BATEXT=1 indicates the presence of a battery, and BATEXT=0 indicates the absence of a battery). Afterwards, clear ENBATDT to 0.

2. If the battery is not connected, there is no need to open Charger. If there is a battery present, configure the charging parameters and finally set the EN_CHG to 1. And then the IC start charging. Try not to modify charging parameters during the charging process, otherwise unexpected situations may occur.

3. After the normal charging is completed, the software does not need to turn off the Charger. The hardware will automatically turn off the Charger (the register remains 1), and detect the battery voltage. When the battery voltage drops below 4.1V again, the hardware will automatically turn on charging again. If the software does not want the battery voltage to drop below 4.1V before restarting charging, the software can set the EN_ CHG to 0 and then set it to 1 to force recharging.

4. If the charging timing function is enabled and the timing time ends, and the battery has not yet reached the target voltage, the charging will end abnormally. And the hardware will generate a maskable interrupt flag and reset the EN_CHG register to 0. The software can prompt the user for abnormal charging, or set EN_CHG to 1 to force charging to start again.

LED Module

IP6303 has a charging status output pin, the CHGLED, can control the blinking behavior of external LED. There are two optional modes as below:

	CHARGE STATUS			
BIT_VAL	Charge	Charge End	Discharge	Low Voltage
0	ON	OFF	OFF	ON-OFF(slow flash)
1	ON-OFF(fast flash)	ON	ON	ON-OFF(slow flash)

ADC

IP6303 integrates 8-BIT Analog-to-Digital Converter (ADC).It can simultaneously detect battery voltage, charging current, operating current and external voltage.

VOLTAGE

Equation：**VBAT = VBATADC*15.625+500+0.5*15.625 (mV)**

DISCHARGE Current

Equation：**IBAT = (IBATADC*15.625-1100+0.5*15.625)/0.495 (mA)**

DCHARGE Current

Equation：**ICHG = (ICHGADC*15.625-750+0.5*15.625)/3 (mA)**

EXTERNAL Voltage

Equation： **VGPx = GPxADC *15.625-500+0.5*15.625 (mV)**

Intelligent Protection

In the ACTIVE state, if the voltage falls below 85% of the required level of any one of the power supply which is enabled and this condition last more than 16ms, the action taken in response to an abnormal power protection can be set. The reaction of this protection can be set by register. Three options will be available including shutting down, reset and ignore.

In the ACTIVE state and STANDBY state, if the VIN voltage rises above the overvoltage protect threshold or falls below the under-voltage protect threshold which are pre-set by register, the action taken in response to the relevant protection can be set and then all the power supplies will be shut down automatically.

In the ACTIVE state and STANDBY state, when the load current of LDO rises above 40% of the capacity level, the corresponding overcurrent flag will be set in the first place. Meanwhile the overcurrent interrupt will be send to the processor if the corresponding interrupt was enabled (can be disabled as well). When the interrupt was received, the processor can take some actions such as lightening or shutting down the load. If the processor cannot take some corresponding measures to this condition within 8ms, the continuous overcurrent condition of the LDOs will trigger the overcurrent protection and all the power supplies will be shut down automatically.

In the ACTIVE state and STANDBY state, if the chip temperature continues to rise, and exceeds the over-temperature protect threshold which is set in the register, the over- temperature protection will be triggered and then all the power supplies will be shut down automatically.

Any one of the protections described above is triggered, the IP6303 will pull down the POR voltage and reset the whole system. The Multi-Functional Peripheral (MFP) will reset to the default state and all the power supplies will be shut down at the same time.

Multiplexing

The detail of the MFP:

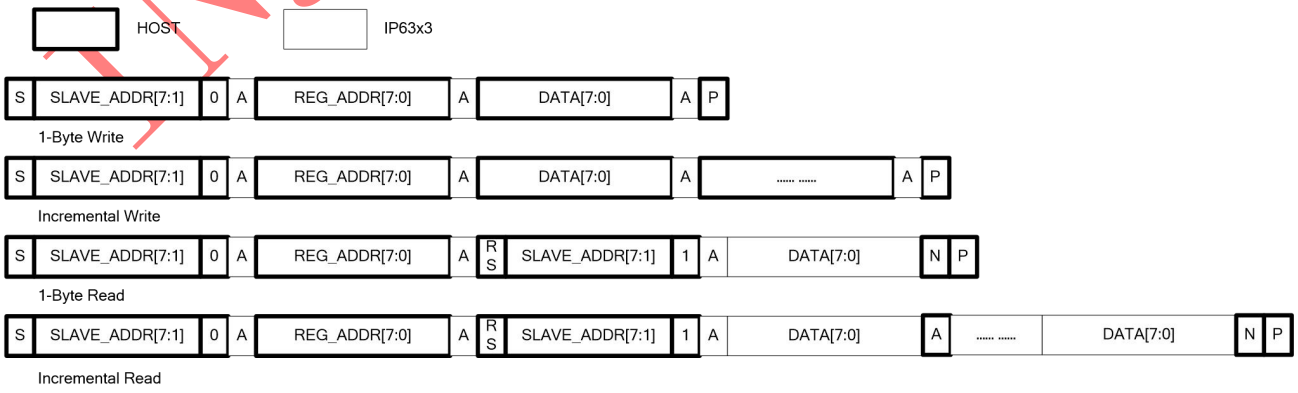
PadName	Func1	Func2	Func3	Func4	Func5
GPIO1	GP1ADC	CHGLED		32K_CLKOUT	GPIO1
CHGLED	CHGLED		GP2ADC		GPIO2
IRQ	IRQ		DCDC1_EN		GPIO3
SCK	SCK	LDO4_EN	CHGLED		GPIO4
SDA	SDA	LDO5_EN			GPIO5
IRQS	WKIRQ				GPIO7
NTC	LDO4OUT		NTC	32K_CLKOUT	GPIO8
LDO5	LDO5OUT			32K_CLKOUT	GPIO9
POR	POR				GPIO10
DC2VSEL	DC2VSEL				GPIO11

* When using the corresponding MFP functions, the corresponding MFP registers must be set, otherwise the unpredictable result may be occurred.

POR and CPUIRQ can both work in Push-Pull or Open-Drain mode.

I2C Interface

A general-purpose serial control interface (I2C) allows read and write access to the configuration registers of all resources of the IP6303. These interfaces support the standard slave mode (100Kbps), fast mode (400Kbps). The IP6303 can support the operations of continuous reading and writing. The default writing slave address is 0x60 and the reading one is 0x61. BIT[3:1] of the address can be rewrite according to the applications.



(S = Start, RS = Repeated Start, A = Acknowledge, N = No Acknowledge , P = Stop)

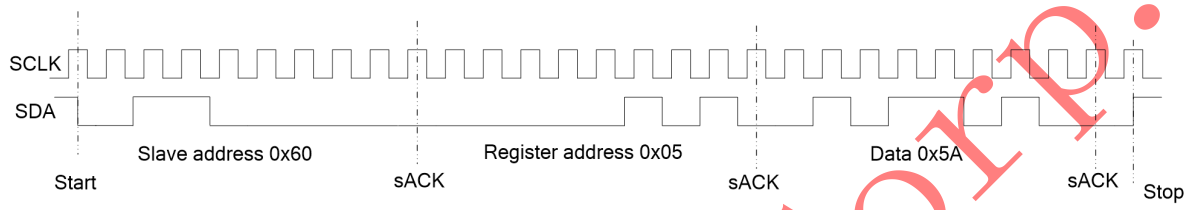
Registers are written to and read from the master through the I2C Interface. The IP6303

I2C acts as slave and is controlled by the master. The SCK line of the I2C interface is driven by the master. The SDA line could be pulled up to VCC by a 1.5Kohm resister and pulled

down by either the master or the slave. A typical WRITE sequence for writing 8bits data to a register is shown in below figures. A start bit is given by the master, followed by the slave address, register address and 8-bit data. After each 8-bit address or data transfered, the IP6303 gives an ACK bit. The master stops writing by sending a stop bit.

All 8 bits data must be written before the register is updated.

Example: Write 8bit data 0x5a to register 0x05, and the slave address is 0X60



Note：Sack generated by Slave, Mack generated by Master, andMnack is a NACK generated by Master

Figure18 I2C WRITE

A typical READ sequence is shown in below figure. First the master has to write the slave address,followed by the register address. Then a restart bit and the slave address specify that a READ is generated. Themaster then clocks out 8 bits at a time to read data.

Example: Read 8bit data 0x5A from register 0x05, and the slave address is
0X60

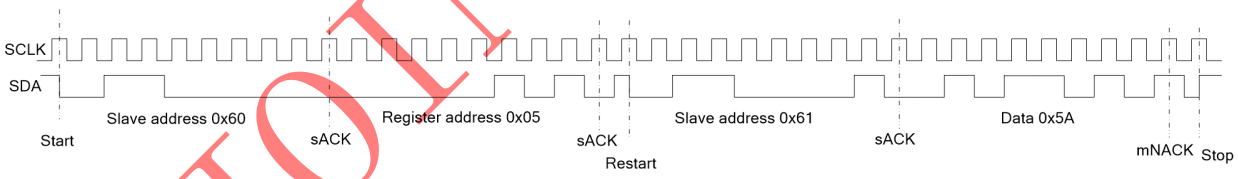


Figure 19 I2C Read

Register

PMU

PSTATE_CTL0(0x00)

Offset = 0x0 default= 0x18

Bit	Name	Description	R/W	Reset[1]
7	ALARM_WKEN	0:disable 1:enable	R/W	0
6	WKIRQ_WKEN	0:disable 1:enable	R/W	0
5	ONOFFL_WKEN	0:disable 1:enable	R/W	0
4	ONOFFS_WKEN	0:disable 1:enable	R/W	1
3	VBUS_WKEN	0:disable 1:enable	R/W	1
2	POR_OFF_EN	0:disable 1:enable	R/W	0
1	INST_PDWN	Power OFF Mode 0: sequence 1: simultaneous	R/W	0
0	POFF_EN	0: RUN 1: SLEEP	R/W	0

PSTATE_CTL1(0x01)

Offset = 0x1 default= 0x01

Bit	Name	Description	R/W	Reset[1]
7	-	-	-	-
6	LDOOCS_EN	0:disable 1:enable	R/W	0
5:4	WKIRQ_POL	WKIRQ polarity selection 00: High Active 01: Low Active 10: Low-to-High edge Active	R/W	00

		11: High-to-Low edge Active		
3	ONOFFUS_WKEN	0:disable 1:enable	R/W	0
2:1	-	-	-	-
0	ONOFF_ULRST_EN	0:disable 1:enable	R/W	1

PSTATE_CTL2 (0x02)

Offset = 0x2 default= 0xA9

Bit	Name	Description	R/W	Reset[2]
7:6	-	-	-	-
5	ENRST	0:disable 1:enable	R/W	1
4	-	-	-	-
3:2	BATOK_SET	BATOK Voltage 00:2.9V 01:3.0V 10:3.1V 11:3.3V	R/W	10
1:0	BATLB_SET	BAT Low Voltage 00:3.2V 01:3.3V 10:3.4V 11:3.5V	R/W	01

PSTATE_CTL3 (0x03)

Offset = 0x3 default= 0x0

Bit	Name	Description	R/W	Reset[2]
7	EN_LDO1PD	0:disable 1:enable	R/W	0
6:1	Reserved	Reserved for analog	R/W	0
0	EN_BATEXT_DT	0:disable 1:enable	R/W	0

PSTATE_SET (0x04)

Offset = 0x4 default= 0x04

Bit	Name	Description	R/W	Reset[1]
7	S2S3_DELAY	POFF_EN mode 0： immediately 1： delay 8ms, OFF	R/W	0
6	POR_S2ON	POR IN S2 0： LOW 1： HIGH	R/W	0
5:4	POFF_TIME	POFF time 00: 0s 01: 1s 10: 2s 11: 4s	R/W	00
3	ONOFF_LRST_TIME	ONOFF_LRST_TIME 0: 6s 1: 10s	R/W	0
2:1	ONOFF_TIME_SET	ONOFF_TIME_SET 00: 1s 01: 2s 10: 3s 11: 4s	R/W	10
0	-	-	-	-

PPATH_CTL (0x05)

Offset = 0x5 default= 0x79

Bit	Name	Description	R/W	Reset[1]
7:2	-	-	-	-
1	EN_BATOC_HOLD	1: enable 0: disable	R/W	0
0	EN_BATOC	1: enable 0: disable	R/W	1

PROTECT_CTL2(0x08)

Offset = 0x8 default= 0x06

Bit	Name	Description	R/W	Reset[1]
7:5	Reserved	Reserved	R/W	000
4	VBUS_UVS_EN	1: enable 0: disable	R/W	0
3	-	-	-	-
2	EN_TEMP	OTP (Over Temperature Protection) 1: ENABLE 0: DISABLE	R/W	1
1:0	VTH_TEMP	Temperature threshold： 11: 150C 10: 135C 01: 120C 00: 105C	R/W	10

PROTECT_CTL3(0x09)

Offset = 0x9 default= 0xCB

Bit	Name	Description	R/W	Reset[1]
7	EN_VBUSOC	1: enable 0: disable	R/W	1
6	EN_VBUSOV	1: enable 0: disable	R/W	1
5	EN_VBUS_UVHD	1: enable 0: disable	R/W	0
4:3	VBUSOC_SET	VBUS OCP interrupt threshold 00: 0.5A 01: 1.0A 10: 1.5A 11: 2.0A	R/W	01
2	OV_SET	VBUSID OVP threshold 1: 6.5 0: 6	R/W	0
1:0	VBUSPU_SET	VBUSID Shut Down Speed 11 FAST 00 SLOW	R/W	11

PROTECT_CTL4(0x0A)

Offset = 0xA default= 0xA4

Bit	Name	Description	R/W	Reset[1]
7:6	EN_VBUSUV_SET	VBUS UVP threshold 00: 3.90V 01: 4.15V 10: 4.50V 11: 4.70V	R/W	10
5:3	VBUSOCH_SET	VBUSID OCP threshold 000: 0.1A 001: 0.5A 010: 0.9A 011: 1.2A 100: 1.5A 101: 1.8A 110: 2.0A 111: disable	R/W	100
2	OK_SET	VBUSID wake up threshold 0:4.0 1:4.3	R/W	1
1	Reserved	Reserved for analog	R/W	0
0	EN_VBUS_5KPD	VBUS 5K PULL DOWN 1: enable 0: disable	R/W	0

PROTECT_CTL5(0x97)

Offset = 0x97 default= 0x55

Bit	Name	Description	R/W	Reset[1]
7:4	Reserved	Reserved for digital	R/W	0101
3	OT_SHUNT_EN	1:enable 0:disable	R/W	0

2	LB_SHUNT_EN	1:enable 0:disable	R/W	1
1	VBUS_OCS_EN	1:enable 0:disable	R/W	0
0	VBUS_OVS_EN	1:enable 0:disable	R/W	1

LDO_OCFLAG (0x0C)

Offset = 0xC default= 0xX

Bit	Name	Description	R/W	Reset[3]
7	LDO7_OCFLAG	1: OC 0: normal	**R**	x
6	LDO6_OCFLAG	1: OC 0: normal	**R**	x
5	LDO5_OCFLAG	1: OC 0: normal	**R**	x
4	LDO4_OCFLAG	1: OC 0: normal	**R**	x
3	LDO3_OCFLAG	1: OC 0: normal	**R**	x
2	LDO2_OCFLAG	1: OC 0: normal	**R**	x
1	-	-	-	-
0	-	-	-	-

DCDC_GOOD (0x0D)

Offset = 0xD default= 0xX

Bit	Name	Description	R/W	Reset[2]
7:4	-	-	-	-
3	DC3_PG	1: DC/DC OK 0: DC/DC disable or Abnormal	R	x
2	DC2_PG	1: DC/DC OK 0: DC/DC disable or Abnormal	R	x
1	DC1_PG	1: DC/DC OK 0: DC/DC disable or Abnormal	R	x
0	-	-	-	-

LDO_GOOD (0x0E)

Offset = 0xE default= 0xX

Bit	Name	Description	R/W	Reset[2]
7	LDO7_PG	1: LDO OK 0: LDO disable or Abnormal	**R**	x
6	LDO6_PG	1: LDO OK 0: LDO disable or Abnormal	**R**	x
5	LDO5_PG	1: LDO OK 0: LDO disable or Abnormal	**R**	x
4	LDO4_PG	1: LDO OK 0: LDO disable or Abnormal	**R**	x
3	LDO3_PG	1: LDO OK 0: LDO disable or Abnormal	**R**	x

2	LDO2_PG	1: LDO OK 0: LDO disable or Abnormal	**R**	x
1	SLDO1_PG	1: LDO OK 0: LDO disable or Abnormal	**R**	x
0	-	-	-	-

PWRON_REC0 (0x10)

Offset = 0x10 default= 0xX

Bit	Name	Description	R/W	Reset[3]
7	WDOG_PON	1 : True 0 : False	R	x
6	ONOFFLRST_PON	1 : True 0 : False	R	x
5	RST_PON	1 : True 0 : False	R	x
4	WKIRQ_PON	1 : True 0 : False	R	x
3	ONOFFUS_PON	1 : True 0 : False	R	x
2	ONOFFS_PON	1 : True 0 : False	R	x
1	ONOFFL_PON	1 : True 0 : False	R	x
0	VBUS_PON	1 : True 0 : False	R	x

PWROFF_REC0 (0x11)

Offset = 0x11 default= 0xX

Bit	Name	Description	R/W	Reset[1]
7	PPOC_POFF	PPATH OCP 1: True 0: False This bit is cleared by writing 1	R/W	X
6	LDOOC_POFF	LDO OCP 1: True 0: False This bit is cleared by writing 1	R/W	X
5	PWROK_POFF	PWROK Protect 1: True 0: False This bit is cleared by writing 1	R/W	X
4	OT_POFF	OTP 1: True 0: False This bit is cleared by writing 1	R/W	X
3	LB_POFF	PPATH Low Power 1: True 0: False This bit is cleared by writing 1	R/W	X
2	WDOG_POFF	Watchdog Reset 1: True 0: False This bit is cleared by writing 1	R/W	X
1	ONOFFRST_POFF	ONOFF Reset 1: True 0: False This bit is cleared by writing 1	R/W	X
0	EN_POFF	POFF_EN 1: True	R/W	X

		0: False This bit is cleared by writing 1		

PWROFF_REC1 (0x12)

Offset = 0x12 default= 0xX

Bit	Name	Description	R/W	Reset[1]
7:2	-	-	-	-
1	POR_EXT_POFF	PWROK Low 1: True 0: False This bit is cleared by writing 1	R/W	X
0	PPOV_POFF	PPATH OVP 1: True 0: False This bit is cleared by writing 1	R/W	X

POFF_LDO (0x18)

Offset = 0x18 default= 0x0

Bit	Name	Description	R/W	Reset[2]
7	LDO7_KEEPON	1: enable 0: disable	R/W	0
6	LDO6_KEEPON	1: enable 0: disable	R/W	0
5	LDO5_KEEPON	1: enable 0: disable	R/W	0

4	LDO4_KEEPON	1: enable 0: disable	**R/W**	0
3	LDO3_KEEPON	1: enable 0: disable	**R/W**	0
2	LDO2_KEEPON	1: enable 0: disable	**R/W**	0
1	SLDO1_KEEPON	1: enable 0: disable	**R/W**	0
0	-	-	-	-

POFF_DCDC (0x19)

Offset = 0x19 default= 0x0

Bit	Name	Description	R/W	Reset[2]
7:4	-	-	-	-
3	DC3_KEEPON	1: enable 0: disable	**R/W**	0
2	DC2_KEEPON	1: enable 0: disable	**R/W**	0
1	DC1_KEEPON	1: enable 0: disable	**R/W**	0
0	-	-	-	-

WDOG_CTL (0x1A)

Offset = 0x1A default= 0x2

Bit	Name	Description	R/W	Reset[3]
7:4	-	-	-	-
3	WDOG_EN	Watchdog Timer 0: disable 1: enable	R/W	0
2	WDOG_CLR	To CLEAR Watchdog Timer Only when it has been written 1, watchdog timer starts to run again.	W	0
1:0	WDOG_TIM	Watchdog time 00: 0.5 s 01: 2 s 10: 8 s 11 :16 s	R/W	10

WDOG_CTL1 (0xFF)

Offset = 0xFF default= 0x26

Bit	Name	Description	R/W	Reset[1]
7	WDOG_SEL	0: old 1: new	R/W	0
6	WDOG_EN_N	New Watchdog Timer 0: disable 1: enable	R/W	0
5:4	WDOG_TIM_N	New Watchdog time 00: 0.5 s 01: 2 s 10: 8 s 11 :16 s	R/W	10
3:1	Reserved	-	R/W	011
0	-	-	R/W	0

LDO_MASK (0x1B)

Offset = 0x1B default= 0x0

Bit	Name	Description	R/W	Reset[3]
7	LDO7_MASK	1: LDO OFF, staying in S1 0: Go to S3	**R/W**	0
6	LDO6_MASK	1: LDO OFF, staying in S1 0: Go to S3	**R/W**	0

5	LDO5_MASK	1: LDO OFF, staying in S1 0: Go to S3	**R/W**	0
4	LDO4_MASK	1: LDO OFF, staying in S1 0: Go to S3	**R/W**	0
3	LDO3_MASK	1: LDO OFF, staying in S1 0: Go to S3	**R/W**	0
2	LDO2_MASK	1: LDO OFF, staying in S1 0: Go to S3	**R/W**	0
1	SLDO1_MASK	1: LDO OFF, staying in S1 0: Go to S3	**R/W**	0
0	-	-	-	-

PWRON_REC1(0x1C)

Offset = 0x1C default= 0xX

Bit	Name	Description	R/W	Reset[3]
7:3	-	-	-	-
2	BATIN_PON	1: True 0: False	R	x
1	ALARM_PON	1: True 0: False	R	x
0	-	-	-	-

DCDC

DC_CTL(0x20)

Offset=0x20 default=0x10

Bit	Name	Description	R/W	Reset[2]
7:6	-	-	-	-
5:3	DC_FRQ	DCDC Frequency: 000~111 0.6MHz~2MHz @ 200KHz step	R/W	010
2	DC3_EN	1: enable 0: disable	R/W	0
1	DC2_EN	1: enable 0: disable	R/W	0
0	DC1_EN	1: enable 0: disable	R/W	0

DC1_VSET(0x21)

Offset=0x21 default=0x20

Bit	Name	Description	R/W	Reset[2]
7:0	DC1_VSET	DC1 Voltage Setting Code: 0000_0000-1111_0000; Value: 0.6-3.6V; Step: 12.5mV 0000_0000 : 0.6V 0010_0000 : 1.0V* 0011_0000 : 1.2V 0100_1000 : 1.5V 1010_0000 : 2.6V V= Vset*12.5mV+0.6V	R/W	0010_0000

DC2_VSET(0x26)

Offset=0x26 default=0x20

Bit	Name	Description	R/W	Reset[2]
7:0	DC2_VSET	DC2 Voltage Setting Code: 0000_0000-1111_0000 / Value: 0.6-3.6V / Step: 12.5mV 0000_0000 : 0.6V 0010_0000 : 1.0V* 0011_0000 : 1.2V 0100_1000 : 1.5V 1010_0000 : 2.6V V= Vset*12.5mV+0.6V	R/W	0010_0000

DC3_VSET(0x2B)

Offset=0x2B default=0xD8

Bit	Name	Description	R/W	Reset[2]
7:0	DC3_VSET	DC3 Voltage Setting Code: 0000_0000-1111_0000 / Value: 0.6-3.6V / Step: 12.5mV 0000_0000 : 0.6V 0010_0000 : 1.0V 0100_1000 : 1.5V 1010_0000 : 2.6V 1100_1000 : 3.1V 1101_1000 : 3.3V V= Vset*12.5mV+0.6V	R/W	1101_1000

LDO

LDO_EN(0x40)

Offset = 0x40 default= 0x0

Bit	Name	Description	R/W	Reset[2]
7	LDO7_EN	LDO 1~7 enable	R/W	0
6	LDO6_EN		R/W	0
5	LDO5_EN		R/W	0
4	LDO4_EN		R/W	0
3	LDO3_EN		R/W	0
2	LDO2_EN		R/W	0
1	SLDO1_EN -		R/W	0
0	-	-	-	-

LDOSW_EN(0x41)

Offset = 0x41 default= 0x01

Bit	Name	Description	R/W	Reset[2]
7	LDO7_EN	LDO 2~7 SWITCH enable	R/W	0
6	LDO6_EN		R/W	0
5	LDO5_EN		R/W	0
4	LDO4_EN		R/W	0
3	LDO3_EN		R/W	0
2	LDO2_EN		R/W	0
1:0	-	-	-	-

LDO2_VSEL(0x42)

Offset = 0x42 default=0x2C

Bit	Name	Description	R/W	Reset[2]
7	-	-	-	-

6:0	LDO2_VSET	LDO2 Voltage Setting Code: 0000000-1101100 | Value: 0.7-3.4 | Step: 25mV 0010000: 1.1V 0101100: 1.8V* 1010100: 2.8V 1100000: 3.1V	R/W	0101100

LDO3_VSEL(0x43)

Offset = 0x43 default=0x2C

Bit	Name	Description	R/W	Reset[2]
7	-	-	-	-
6:0	LDO3_VSET	LDO3 Voltage Setting Code: 0000000-1101100 | Value: 0.7-3.4 | Step: 25mV 0010000: 1.1V 0101100: 1.8V* 1010100: 2.8V 1100000: 3.1V	R/W	0101100

LDO4_VSEL(0x44)

Offset = 0x44 default=0x2C

Bit	Name	Description	R/W	Reset[2]
7	-	-	-	-
6:0	LDO4_VSET	LDO4 Voltage Setting Code: 0000000-1101100 | Value: 0.7-3.4 | Step: 25mV 0010000: 1.1V	R/W	0101100

		0101100: 1.8V* 1010100: 2.8V 1100000: 3.1V		

LDO5_VSEL(0x45)

Offset = 0x45 default=0x48

Bit	Name	Description	R/W	Reset[2]
7	-	-	-	-
6:0	LDO5_VSET	LDO5 Voltage Setting Code: 0000000-1101100 / Value: 0.7-3.4 / Step: 25mV 0010000: 1.1V 0101100: 1.8V 1001000: 2.5V* 1100000: 3.1V	R/W	1001000

LDO6_VSEL(0x46)

Offset = 0x46 default=0x48

Bit	Name	Description	R/W	Reset[2]
7	-	-	-	-
6:0	LDO6_VSET	LDO6 Voltage Setting Code: 0000000-1101100 / Value: 0.7-3.4 / Step: 25mV 0010000: 1.1V 0101100: 1.8V 1001000: 2.5V* 1100000: 3.1V	R/W	1001000

LDO7_VSEL(0x47)

Offset = 0x47 default=0x48

Bit	Name	Description	R/W	Reset[2]
7	-	-	-	-
6:0	LDO7_VSET	LDO7 Voltage Setting Code: 0000000-1101100; Value: 0.7-3.4; Step: 25mV 0010000: 1.1V 0101100: 1.8V 1001000: 2.5V* 1100000: 3.1V	R/W	1001000

LDO_CTL0(0x48)

Offset = 0x48 default= 0X99

Bit	Name	Description	R/W	Reset[1]
7:6	-	-	-	-
5	LDO3_TLEN	1: enable 0: disable	R/W	0
4	LDO3_OCEN	1: enable 0: disable	R/W	1
3:2	-	-	-	-
1	LDO2_TLEN	1: enable 0: disable	R/W	0
0	LDO2_OCEN	1: enable 0: disable	R/W	1

LDO_CTL1(0x49)

Offset = 0x49 default= 0x99

Bit	Name	Description	R/W	Reset[1]
7:6	-	-	-	-
5	LDO5_TLEN	1: enable 0: disable	R/W	0
4	LDO5_OCEN	1: enable 0: disable	R/W	1
3:2	-	-	-	-
1	LDO4_TLEN	1: enable 0: disable	R/W	0
0	LDO4_OCEN	1: enable 0: disable	R/W	1

LDO_CTL2(0x4A)

Offset = 0x4A default= 0x99

Bit	Name	Description	R/W	Reset[1]
7:6	-	-	-	-
5	LDO7_TLEN	0: disable 1: enable	R/W	0
4	LDO7_OCEN	0: disable 1: enable	R/W	1
3:2	-	-	-	-
1	LDO6_TLEN	0: disable 1: enable	R/W	0
0	LDO6_OCEN	0: disable 1: enable	R/W	1

SLDO1_2_VSEL(0x4D)

Offset = 0x4D default=0x25

Bit	Name	Description	R/W	Reset[2]
7:3	SLDO1_VSET	SLDO1 Voltage Setting Code: 00000-11111 / Value: 0.7-3.8 / Step: 0.1V 00100: 1.1V	R/W	00100

		01011: 1.8V*		
2:0	SLDO0_VSET	SLDO0(SVCC) Voltage Setting Code: 000-111 / Value: 2.6-3.3 / Step: 0.1V 101: 3.1V 111: 3.3V*	R/W	101

Charger

CHG_ANA_CTL0(0x50)

Offset = 0x50 default= 0x2D

Bit	Name	Description	R/W	Reset[1]
7:6	R_VCHG_SET	CV Voltage Setting: 11：4.4 10：4.35 01：4.3 00：4.2	R/W	00
5:4	R_CV	Fine Tuning: 11：Add 42mv 10：Add 28mv 01：Add 14mv 00：Add 0mv	R/W	10
3	EN_VILP	1: ENABLE 0: DISABLE	R/W	1
2	EN_IBUSLP	1: ENABLE 0: DISABLE	R/W	1
1	EN_TSLP	1: ENABLE 0: DISABLE	R/W	0
0	EN_ISTOP	1: ENABLE 0: DISABLE	R/W	1

CHG_ANA_CTL1(0x51)

Offset = 0x51 default= 0x26

Bit	Name	Description	R/W	Reset[1]
7	-	-	-	-
6:4	ISET_VBUS	VBUS Charger OCP Threshold： 000：0.1A 001：0.5A 010：0.9A 011：1.3A 100：1.7A 101：2.1A 110：2.5A 111：2.9A	R/W	010
3:2	R_VIL	VOUT Charger UVP Threshold： 11：4.80V 10：4.60V 01：4.25V 00：4.00V	R/W	01
1:0	R_ISTOP	Battery FULL current 11：150mA 10：100 mA 01：62 mA 00：21mA	R/W	10

CHG_DIG_CTL0(0x53)

Offset = 0x53 default=0xD7

Bit	Name	Description	R/W	Reset[2]
7	EN_CHGTIME	Charger CC+CV time： 1：enable 0：disable	R/W	1
6	EN_CVTIME	Charger CV time：	R/W	1

		1：enable 0：disable		
5	-	-	-	-
4:0	R_CHGIS<4: 0>	Charger current ： Code / 电流 / Step 00000-10111 / 25mA-600mA / 25mA 11000-11111 / 650mA-1000mA / 50mA	R/W	10111

CHG_ DIG_CTL1 (0x54)

Offset = 0x54 default= 0xX

Bit	Name	Description	R/W	Reset[1]
7:5	CHG_STATE[2:0]	000: IDLE 001: TK 010: CC 011: ** 100: ** 101: CHG_END 110: Over Time	R	x
4	CHGOP		R	x
3	CHG_END		R	x
2	CV_OV_TIME		R	x
1	CHG_ OV_TIME		R	x
0	TK_ OV_TIME		R	x

CHG_DIG_CTL2(0x55)

Offset = 0x55 default= 0xX

Bit	Name	Description	R/W	Reset[2]
7:4	-	-	-	-
3	BATEXT_OK	Battery Exist 1: True	R	x

		0: False		
1:0	-	-	-	-

NTC_ANA_CTL(0x56)

Offset = 0x56 default= 0x0

Bit	Name	Description	R/W	Reset[2]
7:3			R/W	0
2	NTC_MOD	Current output mode NTC enable 1: enable 0: disable	R/W	0
1	EN_DTSC	Detect NTC pin short circuit enable 1: enable 0: disable	R/W	0
0	EN_NTC	1: enable 0: disable	R/W	0

NTC_DIG_CTL(0x57)

Offset = 0x57 default= 0x0

Bit	Name	Description	R/W	Reset[2]
7:2			R/W	0
1	EN_NTCChg	NTC high/low temperature shutdown charger enable 1: enable 0: disable	R/W	0
0	EN_NTCID	NTC high temperature shutdown BAT ID enable 1: enable 0: disable	R/W	0

CHG_DIG_CTL3(0x58)

Offset = 0x58 default= 0x0

Bit	Name	Description	R/W	Reset[2]
7:3	-	-	-	-
2	CHGLED_MODE	Charge Status 1：Mode1 0：Mode2	R/W	0
1	CHG_EN	Charger enable 1: enable 0: disable	R/W	0
0	-	-	-	-

ADC

ADC_ANA_CTL0(0x60)

Offset = 0x60 default=0x40

Bit	Name	Description	R/W	Reset[3]
7:6	-	-	-	01
5	-	-	-	-
4	GP2_ADC_EN	1: enable 0: disable	R/W	0
3	GP1_ADC_EN	1: enable 0: disable	R/W	0
2	ICHG_ADC_EN	1: enable 0: disable	R/W	0
1	IBAT_ADC_EN	1: enable 0: disable	R/W	0
0	VBAT_ADC_EN	ADC enable， 1: enable 0: disable	R/W	0

Note: 0x60[7:6]=01, do not modify without authorization!

ADC_DATA_VBAT(0x64)

Offset = 0x64 default=0x00

Bit	Name	Description	R/W	Reset[3]
7:0	ADC_DATA_VBAT		R	0

ADC_DATA_IBAT(0x65)

Offset = 0x65 default=0x00

Bit	Name	Description	R/W	Reset[3]
7:0	ADC_DATA_IBAT		R	0

ADC_DATA_ICHG(0x66)

Offset = 0x66 default=0x00

Bit	Name	Description	R/W	Reset[3]
7:0	ADC_DATA_ICHG		R	0

ADC_DATA_GP1(0x67)

Offset = 0x67 default=0x00

Bit	Name	Description	R/W	Reset[3]
7:0	ADC_DATA_GP1		R	0

ADC_DATA_GP2(0x68)

Offset = 0x68 default=0x00

Bit	Name	Description	R/W	Reset[3]
7:0	ADC_DATA_GP2		R	0

INTS/MFP

INTS_CTL (0x70)

Offset = 0x70 default= 0x01

Bit	Name	Description	R/W	Reset[2]
7:1	-	-	-	-
0	CPUIRQ_POL	CPUIRQ polarity selection 1: High Active 0: Low Active	R/W	1

INT_FLAG0 (0x71)

Offset = 0x71 default= 0xX

Bit	Name	Description	R/W	Reset[3]
7	ALARM_PENDING	ALARM pending 1: True 0: False	R/W	0
6	-	-	-	-
5	LB_PENDING	BAT LOW pending 1: True 0: False	R/W	0
4	VBUSOUT_PENDING	VBUS OUT 1: True 0: False	R/W	0
3	VBUSPLUG_PENDING	VBUS IN 1: True 0: False	R/W	0
2	ONOFF_US_PENDING	ONOFF Super Short 1: True 0: False	R/W	0
1	ONOFF_L_PENDING	ONOFF Long 1: True 0: False	R/W	0

0	ONOFF_S_PENDING	ONOFF Short 1: True 0: False	R/W	0

This bit is cleared by writing 1

INT_FLAG1 (0x72)

Offset = 0x72 default= 0xX

Bit	Name	Description	R/W	Reset[3]
7:6	-	-	-	-
5	ONOFF_FLAG	ONOFF Status 0: NOT Press 1: Press	R	x
4	VBUSIN_FLAG	VBUSIN 0: False 1: True	R	0
3	LDOOC_FLAG	LDO OCP 0: False 1: True	R	0
2	-	-	-	-
1	ADCKEY_PENDING	ADCKEY 0: False 1: True	R/W	0
0	HT_PENDING	High Temperature 0: False 1: True	R/W	0

INT_MASK0 (0x73)

Offset = 0x73 default= 0xFF

Bit	Name	Description	R/W	Reset[3]
7	ALARM_MASK	ALARM interrupt mask 0: enable 1: disable	R/W	1

6	-	-	-	-
5	LB_MASK	BAT LOW interrupt mask 0: enable 1: disable	R/W	1
4	VBUSOUT_MASK	VBUS PLUGOUT interrupt mask 0: enable 1: disable	R/W	1
3	VBUSPLUG_MASK	VBUS PLUGIN interrupt mask 0: enable 1: disable	R/W	1
2	ONOFF_US_MASK	ONOFF Super Short interrupt mask 0: enable 1: disable	R/W	1
1	ONOFF_L_MASK	ONOFF Long interrupt mask 0: enable 1: disable	R/W	1
0	ONOFF_S_MASK	ONOFF Short interrupt mask 0: enable 1: disable	R/W	1

INT_MASK1 (0x74)

Offset = 0x74 default= 0x1F

Bit	Name	Description	R/W	Reset[3]
7:5	-	-	-	-
4	VBUSIN_MASK	VBUS interrupt mask 0: enable 1: disable	R/W	1
3	LDOOC_MASK	LDO OCP interrupt mask 0: enable 1: disable	R/W	1
2	-	-	-	-
1	ADCKEY_MASK	ADCKEY interrupt mask	R/W	1

		0: enable 1: disable		
0	HT_MASK	High Temperature interrupt mask 0: enable 1: disable	R/W	1

MFP_CTL0 (0x75)

Offset = 0x75 default= 0x03

Bit	Name	Description	R/W	Reset[2]
7	-	-	-	-
6:5	IO3_MFP	IO3 MFP 00: IRQ* 01: ---- 10: DCDC1_EN 11: GPIO3	R/W	00
4:3	IO2_MFP	IO2 MFP 00: CHGLED* 01: ---- 10: GP2ADC 11: GPIO2	R/W	00
2:0	IO1_MFP	IO1 MFP 000: GP1ADC 001: CHGLED 010: ---- 011: GPIO1* 100: 32K 101-111: Reserved	R/W	011

MFP_CTL1 (0x76)

Offset = 0x76 default= 0x0

Bit	Name	Description	R/W	Reset[2]

7:6	IO8_MFP	IO8 MFP 00: LDO4OUT* 01: 32K 10: NTC 11: GPIO8	R/W	00
5:4	IO7_MFP	IO7 MFP 00: WKIRQ* 01: Reserved 10: Reserved 11: GPIO7	R/W	00
3:2	IO5_MFP	IO5 MFP 00: SDA* 01: LDO5_EN 10: ---- 11: GPIO5	R/W	00
1:0	IO4_MFP	IO4 MFP 00: SCK* 01: LDO4_EN 10: CHGLED 11: GPIO4	R/W	00

MFP_CTL2 (0x77)

Offset = 0x77 default= 0x0

Bit	Name	Description	R/W	Reset[2]
7:4	-	-	-	-
5:4	IO11_MFP	IO11 MFP 00: DC2VSEL* 01: ---- 10: ---- 11: GPIO11	R/W	00
3:2	IO10_MFP	IO10 MFP 00: POR* 01: ----	R/W	00

		10: ---- 11: GPIO10		
1:0	IO9_MFP	IO9 MFP 00: LDO5OUT* 01: 32K 10: ---- 11: GPIO9	R/W	00

GPIO_OE0 (0x78)

Offset = 0x78 default= 0x0

Bit	Name	Description	R/W	Reset[2]
7:1	GPIO_OE	GPIO1~7 Output Enable 0: disable 1: enable	R/W	0
0	-	-	-	-

GPIO_OE1(0x79)

Offset = 0x79 default= 0x0

Bit	Name	Description	R/W	Reset[2]
7:4	-	-	-	-
3	GPIO_OE	GPIO11 Output Enable 0: disable 1: enable	R/W	0
2	GPIO_OE	GPIO10 Output Enable 0: disable 1: enable	R/W	0
1	GPIO_OE	GPIO9 Output Enable 0: disable 1: enable	R/W	0
0	GPIO_OE	GPIO8 Output Enable 0: disable	R/W	0

		1: enable		

GPIO_IE0 (0x7A)

Offset = 0x7A default= 0x0

Bit	Name	Description	R/W	Reset[2]
7:1	GPIO_IE	GPIO1~7 Input Enable 0: disable 1: enable	R/W	0
0	-	-	-	-

GPIO_IE1 (0x7B)

Offset = 0x7B default= 0x0

Bit	Name	Description	R/W	Reset[2]
7:4	-	-	-	-
3	GPIO_IE	GPIO11 Input Enable 0: disable 1: enable	R/W	0
2	GPIO_IE	GPIO10 Input Enable 0: disable 1: enable	R/W	0
1	GPIO_IE	GPIO9 Input Enable 0: disable 1: enable	R/W	0
0	GPIO_IE	GPIO8 Input Enable 0: disable 1: enable	R/W	0

GPIO_DAT0(0x7C)

Offset = 0x7C default= 0x0

Bit	Name	Description	R/W	Reset[2]
7:1	GPIO_DAT	GPIO1~7 Data	R/W	0
0	-	-	-	-

GPIO_DAT1 (0x7D)

Offset = 0x7D default= 0x0

Bit	Name	Description	R/W	Reset[2]
7:4	-	-	-	-
3	GPIO_DAT	GPIO11 Data	R/W	0
2	GPIO_DAT	GPIO10 Data	R/W	0
1	GPIO_DAT	GPIO9 Data	R/W	0
0	GPIO_DAT	GPIO8 Data	R/W	0

PAD_PU0(0x7E)

Offset = 0x7E default= 0x0

Bit	Name	Description	R/W	Reset[3]
7:1	GPIO_PU	0: disable 1: enable	R/W	0
0	-	-	-	-

PAD_PU1(0x7F)

Offset = 0x7F default= 0x0

Bit	Name	Description	R/W	Reset[3]
7:4	-	-	-	-
3	GPIO_PU	0: disable 1: enable	R/W	0
2	GPIO_PU	0: disable 1: enable	R/W	0

1	GPIO_PU	0: disable 1: enable	R/W	0
0	GPIO_PU	0: disable 1: enable	R/W	0

PAD_PD0 (0x80)

Offset = 0x80 default= 0x0

Bit	Name	Description	R/W	Reset[3]
7:1	GPIO_PD	0: disable 1: enable	R/W	0
0	-	-	-	-

PAD_PD1(0x81)

Offset = 0x81 default= 0x0

Bit	Name	Description	R/W	Reset[3]
7:4	-	-	-	-
3	GPIO_PD	0: disable 1: enable	R/W	0
2	GPIO_PD	0: disable 1: enable	R/W	0
1	GPIO_PD	0: disable 1: enable	R/W	0
0	GPIO_PD	0: disable 1: enable	R/W	00

PAD_CTL(0x82)

Offset = 0x82 default= 0x00

Bit	Name	Description	R/W	Reset[1,2]
7:4	-	-	-	-

3	CPUIRQ_PAD	CPUIRQ PAD Mode 0: Push-pull 1: Open-drain	R/W	0 (RST1)
2	POR_PAD	POR PAD Mode 0: Push-pull 1: Open-drain	R/W	0 (RST1)
1:0	-	-	-	-

INT_PENDING0(0x83)

Offset = 0x83 default= 0x0

Bit	Name	Description	R/W	Reset[3]
7	LDO7_OCPENDING	0: None 1: INT pending	**R/W**	0
6	LDO6_OCPENDING	0: None 1: INT pending	**R/W**	0
5	LDO5_OCPENDING	0: None 1: INT pending	**R/W**	0
4	LDO4_OCPENDING	0: None 1: INT pending	**R/W**	0
3	LDO3_OCPENDING	0: None 1: INT pending	**R/W**	0
2	LDO2_OCPENDING	0: None 1: INT pending	**R/W**	0
1:0	-	-	-	-

This bit is cleared by writing 1

INT_PENDING1 (0x84)

Offset = 0x84 default= 0x0

Bit	Name	Description	R/W	Reset[3]	T
7:3	-	-	-	-	
2	BATOC_PENDING	0: None 1: INT pending	R/W	0	D
1	VBUSUV_PENDING	0: None 1: INT pending	R/W	0	D
0	VBUSOC_PENDING	0: None 1: INT pending	R/W	0	D

This bit is cleared by writing 1

I2C

ADDR_CTL(0x99)

Offset = 0x99 default=0x60

Bit(s)	Name	Description	R/W	Reset[2]
7:4	ADDR	Slave device address	R	0110
3:1	ADDR	Slave device address	R/W	000
0	-	-	-	-

RTC

RTC_CTL(0xA0)

Offset = 0xA0 default=0x13

Bit(s)	Name	Description	R/W	Reset
7:2	-	-	-	-
1	RTCE	0: disable 1: enable	R/W	1
0	RST	RTC Reset	R/W	1

RTC_SEC_ALM(0xA1)

Offset =0xA1 default 0x00

Bit(s)	Name	Description	R/W	Reset
7:6	-	-	R	0
5:0	SECAL	Alarm second setting 00H – 3BH	R/W	0

RTC_MIN_ALM(0xA2)

Offset = 0xA2 default 0x00

Bit(s)	Name	Description	R/W	Reset
7:6	-	-	R	0
5:0	MINAL	Alarm minute setting 00H – 3BH	RW	0

RTC_HOUR_ALM(0xA3)

Offset = 0xA3 default 0x00

Bit(s)	Name	Description	R/W	Reset
7:5	-	-	R	0
4:0	HOUEAL	Alarm hour setting 00H – 17H	R/W	0

RTC_DATE_ALM(0xA4)

Offset =0xA4 default 0x00

Bit(s)	Name	Description	R/W	Reset
7:5	-	-	R	0
4:0	DATEAL	Alarm day setting 01H – 1FH	R/W	0

RTC_MON_ALM(0xA5)

Offset = 0xA5 default 0x00

Bit(s)	Name	Description	R/W	Reset
7:4	-	-	R	0
3:0	MONAL	Alarm month setting 01H – 0CH	R/W	0

RTC_YEAR_ALM(0xA6)

Offset =0xA6 default 0x00

Bit(s)	Name	Description	R/W	Reset
7	-	-	R	0
6:0	YEARAL	Alarm year setting 00H – 63H	R/W	0

RTC_SEC(0xA7)

Offset = 0xA7 default 0x00

Bit(s)	Name	Description	R/W	Reset
7:6	-	-	R	0
5:0	SECAL	Time second setting 00H – 3BH	R/W	0

RTC_MIN(0xA8)

Offset =0xA8 default 0x00

Bit(s)	Name	Description	R/W	Reset
7:6	-	-	R	0
5:0	MINAL	Time minute setting 00H – 3BH	R/W	0

RTC_HOUR(0xA9)

Offset = 0xA9 default 0x00

Bit(s)	Name	Description	R/W	Reset
7:5			R	0
4:0	HOUEAL	Time hour setting 00H – 17H	R/W	0

RTC_DATE(0xAA)

Offset = 0xAA default 0x01

Bit(s)	Name	Description	R/W	Reset
7:5	-	-	R	0
4:0	DATEAL	Time day setting 01H – 1FH	R/W	00001

RTC_MON(0xAB)

Offset = 0xAB default 0x11

Bit(s)	Name	Description	R/W	Reset
7	-	-	R	0
6:4	DAY	Time day setting 01H – 07H	R/W	001
3:0	MONAL	Time month setting 01H – 0CH	R/W	0001

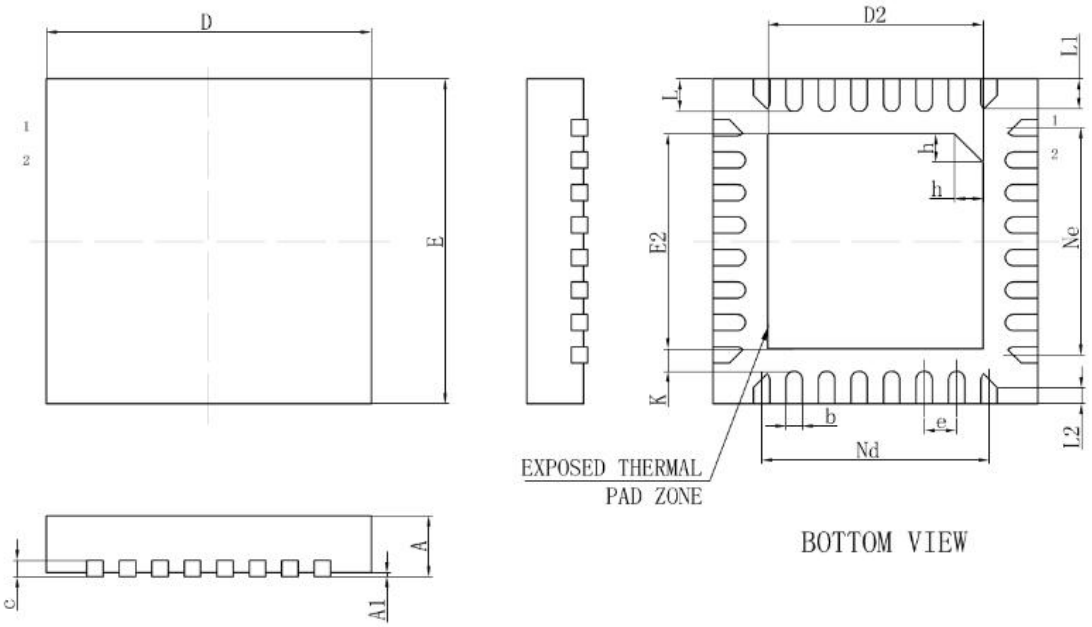
RTC_YEAR(0xAC)

Offset = 0xAC default 0x00

Bit(s)	Name	Description	R/W	Reset
7	LEAP	RTC Leap Year bit 1: leap year	R	0

		0: not leap year		
6:0	YEARAL	Time year setting 00H – 63H	R/W	0

Package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
Ne	2.80BSC		
K	0.20	-	-
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40
上/下载体尺寸 (MIL)	112*112		

Important Notice

INJOINIC TECHNOLOGY Corp. and its subsidiaries reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to INJOINIC TECHNOLOGY Corp.'s terms and conditions of sale supplied at the time of order acknowledgment.

INJOINIC TECHNOLOGY Corp. assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using INJOINIC's components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of INJOINIC's components in its applications, notwithstanding any applications-related information or support that may be provided by INJOINIC. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify INJOINIC TECHNOLOGY and its representatives against any damages arising out of the use of any INJOINIC's components in safety-critical applications.

Reproduction of significant portions of INJOINIC's information in INJOINIC's data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. INJOINIC TECHNOLOGY Corp. is not responsible or liable for such altered documentation. Copying information from third parties may be subject to additional restrictions.

INJOINIC will update this document from time to time. The actual parameters of the product may vary due to different models or other items. This document is not a warranty of any kind, express or implied.

Resale of INJOINIC's components or services with statements different from or beyond the parameters stated by INJOINIC for that component or service voids all express and any implied warranties for the associated INJOINIC's component or service and is an unfair and deceptive business practice. INJOINIC TECHNOLOGY Corp. is not responsible or liable for any such statements.